33-1253 Technical description:

Introduction:

The 33-1253 consists of a 2.4GHz dongle and a 2.4GHz headphone. Any analog music source that is applied to the dongle will be sent to the headphone via 2.4GHz RF link without any compression. The audio being sent by the dongle will be reproduced at the headphone side.

Dongle operation:

The role of the dongle is to accept any analog audio input and transmit the audio data to the corresponding headphone.

ADC:

The audio encoding is done by the ADC chip uDA1361TS (U4). The uDA1361TS is a single chip stereo analog-to-digital converter employing bit-stream conversion techniques. The ADC chip is set to master mode and system clock apply to the chip is about 11.29MHz (fsys). Therefore the sampling frequency is 44.1KHz (fsys/256) and with a resolution of 16 bit digital data.

2.4GHz wireless audio streamer:

The digital data will then be sent to the 2.4GHz wireless audio streamer chip nRF24Z1 (U1). U1 works as an 2.4GHz RF transceiver with 4MBit/S data rate. It handles audio I/O, RF protocol and RF link management. The EEPROM chip (U2) stores the initial configuration of the U1. Once the unit is powered on, U1 goes into a power on reset, and the reset is held until the supply voltage is kept higher than the minimum operation voltage (2V) for a few millisecond. When the reset is released, the chip needs to be configured. It will look for the external EEPROM (U2) memory on the SPI master interface. Then configuration data is load from U2. Once U1 is configured, it starts the link-locate state that the dongle will try to establish link with the corresponding headphone by iteratively sending short search packages on all available channels until acknowledge is received from the corresponding headphone. Once the acknowledge is received, the dongle will enter the synchronization state. This synchronization state takes care of synchronizing the channel hopping engine on dongle and headphone, to secure that both parts follows the same hopping sequence. Which channel to start from is implicitly found during the link-locate state. When the dongle and headphone are in synchronization mode, the audio stream formats are converted to the nRF24Z1 RF protocol and transferred over the air.

Power step up:

The operation voltage is kept at 2.5V by a step up chip XC6371C251PR (U6) that is supplied by battery voltage.

Low battery:

The battery monitor chip XC61CN2002MR/BU4820 (U9) that connects its input to the battery, works as a 2V battery monitor chip. When the battery voltage drops below 2V, it's output will be dropped from Vdd (2.5V) to zero volt. Then the ADC chip (U4) is powered down and the LED (D3) will also be turned off.

Battery charging for both dongle and headphone:

Once the charging hub (provided) is connected to the power jack of either the dongle or the headphone. The battery voltage is disconnected from the main circuit and therefore the unit can not be operated when it is charging.

32-1253 uses a single chip transceiver IC from Nordic nRF24Z1.

RF PART

The single chip transceiver IC contains all necessary RF circuit. It converts the RF FSK signal picked up by the antenna for further processing. Besides, the base band digital signal, including voice and commands, will be modulated to FSK format on the RF carrier during transmission. The main building blocks of the RF parts includes a LNA, Mixer, IF Band pass filter, VCO with frequency synthesiser, RF power amplifier for transmission. Among those building blocks, the RF circuit can be divided into two sections.

A: RX section

This product employs traditional single conversion architecture with the following functional blocks:

1. The LNA has low noise figure and high insertion gain.
2. The LO signal is generated VCO and the LO frequency is controlled by the frequency synthesizer after received command from external MCU.
3. The mixer is to convert RF signal to an IF signal. This IF signal will further filter by the IF band pass filter.
4. The IF signal is then down converted to digital signals, i.e. CLK and DATA.
5. The digital DATA is further convert to analogue voice signal through the external DAC IC.

B: TX section

1. The digital DATA is from the external ADC and it is applied to the transceiver IC.
2. It is further filtered by the GFSK filter before going to the VCO and the frequency of transmission is controlled by the frequency synthesizer.
3. The FSK modulated signal is amplified by the internal PA.
4. The amplified RF signal is applied to the antenna with the external matching circuit.