

# Nimbus 220

**Data sheet** 





### **Document information**

This document defines the module reference design and its air and hardware interfaces for customer applications. It can help customers quickly understand the hardware interface specifications, electrical characteristics, mechanical specifications, and other related information of the Nimbus 220 module reference design. With the assistance of this document, coupled with application manuals and user guides, customers can quickly apply the Nimbus 220 module reference design to wireless applications.

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## 1. Functional description

#### 1.1. Overview

Nimbus 220 is a NB-IoT module that supports the Upper 700 MHz A Block spectrum, which has been standardized by 3GPP for NB-IoT and designated as LTE Band 103. This band is utilized in energy, electric and gas utility, transportation, and other industries. Several other bands are also supported, as shown by the feature list in this document. The module's compact size (18 mm x 16 mm x 2.4 mm), LCC package, and wide power supply range make it easily embeddable and compatible with a wide range of applications.

Nimbus 220 is a high-performance LTE Cat NB2 module with ultra-low power consumption compliant with 3GPP release 14. It supports a wide range of IP-based protocols, including UDP, TCP, CoAP, LwM2M, MQTT, TLS, DTLS, SNTP and HTTP. Nimbus 220 is a power-optimized product that delivers 10+ years of device's battery life.

Nimbus 220, with its advanced feature set and support for Upper 700 MHz A Block (3GPP band 103), is recommended for developing new long-range, low-power IoT applications, as well as for migrating from other legacy cellular or unlicensed technologies, for industries such as utilities, smart grids, AMI, transportation, and others.

### 1.2. Product features

The Nimbus 220 module reference design is a high-performance, low-power NB-IoT series module. Through the NB-IoT radio communication protocol (3GPP Release 13 and Release 14), the Nimbus 220 module can establish communication with the network operator's infrastructure equipment.

The frequency bands supported by the Nimbus 220 module are displayed in the table below.

Duplex mode	Frequency band
HD-FDD	13/103

Table 1: Frequency bands supported by the module

The table below describes the main features of the Nimbus 220 module in detail.

Description	Value

v.1.0 b103 5



Voltage	Supply voltage range: 2.97 V – 3.63 V Nominal supply voltage: 3.3 V
Power consumption in power saving mode (PSM)	PSM nominal power consumption 2.5 μA PSM maximum power consumption 4 μA
Standards	LTE Cat NB1 / NB2
Transmit power	23 dBm ± 2 dB
Frequency band	13/103
USIM interface	1.8 V and 3.0 V
Main serial port	After the module is turned on, it is in the adaptive serial transmission rate mode by default (supports self-adjusting synchronization of serial transmission rates below 115,200 bps)  The MCU must continually send AT commands to the module in order to synchronize the serial transmission rate, and it will return "OK" to indicate successful synchronization  After waking up from sleep mode, the module will directly use the serial transmission rate that has been successfully synchronized after power-on, without requiring resynchronization
Debug serial port	Used for software debugging to obtain underlying logs. Default serial port rate: 115,200 bps
Auxiliary serial port	Used for software debugging to obtain underlying logs. Default serial port rate: 115,200 bps
Internet protocol	UDP/TCP/COAP/LwM2M/TLS/DTLS/ SNTP/MQTT/HTTP
SMS	Text and PDU modes



Data rate characteristics	Single-tone: 25.5 kbps (downlink), 16.7 kbps (uplink) Multitone: 25.5 kbps (downlink), 62.5 kbps (uplink)
AT command	AT commands defined by 3GPP TS 27.005, 27.007
Description	Value
Firmware upgrade	Upgrade via main serial port or FOTA (Firmware Over-the-Air)
Physical characteristics	Dimensions: $(17.85 \pm 0.15) \text{ mm} \times (15.85 \pm 0.15) \text{ mm} \times (2.4 \pm 0.2) \text{ mm}$ Weight: $1.2 \text{ g} \pm 0.2 \text{ g}$
Temperature range	Normal operating temperature: -25 °C - +75 °C¹ Extended operating temperature: -30 °C - +85 °C² Storage temperature: -40 °C - +90 °C
Antenna interface	50 Ω characteristic impedance
RoHS	Fully EU RoHS compliant

Table 2: Main features of the Nimbus 220 module

### 1.3. Functional block diagram

The following figure is a functional block diagram illustrating the main functions of the design:

RF part

<sup>&</sup>lt;sup>1</sup> It means that when the module operates within this temperature range, its performance is compliant with the 3GPP standard.

<sup>&</sup>lt;sup>2</sup> It means that when the module operates in this temperature range, it can still maintain a normal operating state with functions such as SMS and data transmission; there will be no irrecoverable faults; the radio frequency spectrum and the network will not be significantly affected. Only the values of individual parameters, such as output power, may exceed the scope of 3GPP standards. When the temperature returns to the normal operating temperature range, the indicators of the module still comply with the 3GPP standard.



- Baseband part
- Power management
- Peripheral interface

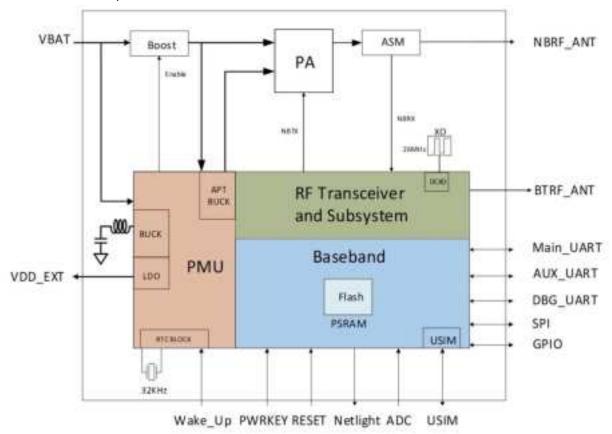


Figure 1: Functional block diagram

## 2. Interfaces

The Nimbus 220 module has a total of forty (40) LCC pins. Subsequent chapters elaborate upon the following functions and interfaces of the module:

- PSM
- Power supply
- RESET
- CHIP ENB
- WAKE UP
- Serial port
- SPI interface
- USIM interface



- ADC interface<sup>3</sup>
- Network Status Indicator⁴

   Antenna interface

### 2.1. Pin assignment

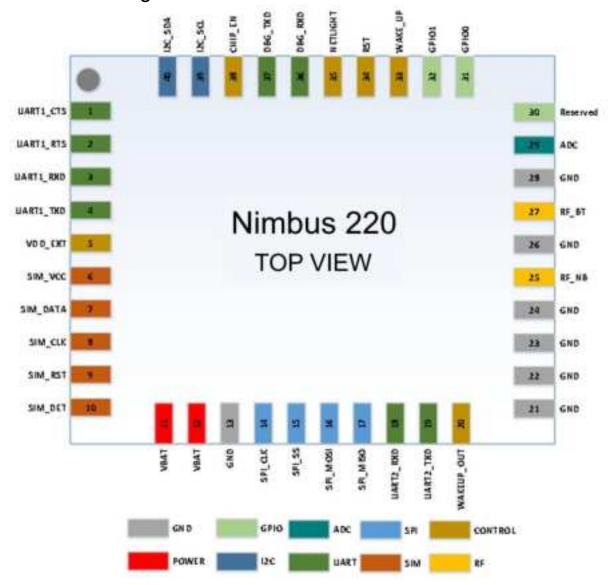


Figure 2: Pin assignment diagram<sup>5</sup>

### 2.2. Pin description

The following table describes the pin definitions of the Nimbus 220 module in detail.

<sup>&</sup>lt;sup>3</sup> Under development

<sup>&</sup>lt;sup>4</sup> Under development

<sup>&</sup>lt;sup>5</sup> Leave all reserved pins open



Туре	Description
IO	Bidirectional port
Туре	Description
DI	Digital input
DO	Digital output
PI	Power input
PO	Power output
Al	Analog input
AO	Analog output

Table 3: I/O parameter definitions

Power supply					
Pin name	Pin number	I/O	Description	DC characteristics	Remarks
VBAT	11, 12	PI	Module power supply	V max = 3.63 V V min = 2.97 V V norm = 3.3 V	
VDD_EXT	5	PO	1.8 V output power supply	Vnorm = 1.8 V	There is no voltage output in PSM mode. It can supply power for the pull-up circuit of the module; it is not recommended for external circuit power supply



GND	13, 21, 22, 23, 24, 26, 28	GND				
Power butto	on interfac	е				
Pin name	Pin number	I/O	Description	DC characteristics	Remarks	
CHIP_ENB	38	DI	Pull down CHIP_ENB to power on the module	$V_{IL}$ max = 0.3 * VBAT $V_{IH}$ min = 0.7 * VBAT	Can be used as a PowerKey	
Reset interf	ace					
Pin name	Pin number	I/O	Description	DC characteristics	Remarks	
RESET	34	DI	Reset module		Active low	
WAKE_UP i	nterface					
Pin name	Pin number	I/O	Description	DC characteristics	Remarks	
WAKE_UP	33	DI	External interrupt pin. Wake up the module from PSM		Active low	
WAKEUP_C	WAKEUP_OUT interface					
Pin name	Pin number	I/O	Description	DC characteristics	Remarks	



WAKEUP_ OUT	20	DO	Control external circuit switch		1.8 V domain and be sure to respect the end specification
Network sta	tus indica	tor			
Pin name	Pin number	I/O	Description	DC characteristics	Remarks
NETLIGHT	35	DO	Network status indicator		1.8 V domain and be sure to respect the end specification
ADC interfa	ce				
Pin name	Pin number	I/O	Description	DC characteristics	Remarks
ADC	29	Al	Universal	Voltage range:	
			Analog-to-Digital Conversion Interface	0 V – 5 V	
Main serial	port				
Pin name	Pin number	I/O	Description	DC characteristics	Remarks
UART1_RXD	3	DI	Receive data		4.0.1/
UART1_TXD	4	DO	Send data		1.8 V voltage domain, and be sure to follow the end
UART1_RTS	2	DO	Send data		specification
UART1_CTS	1	DI	Receive data		



Debug seria	al port				
Pin name	Pin number	I/O	Description	DC characteristics	Remarks
DBG_RXD	36	DI	Receive data		
DBG_TXD	37	DO	Send data		1.8 V voltage domain, and be sure to follow the end specification
Auxiliary se	rial port				
Pin name	Pin number	I/O	Description	DC characteristics	Remarks
UART2_RXD	18	DI	Receive data		
UART2_TXD	19	DO	Send data		3.3V voltage domain, and be sure to follow the end specification
GPIO & Res	erved				
Pin name	Pin number	I/O	Description	DC characteristics	Remarks
GPIO0	31	Ю	GPIO	In all usage states, the input voltage must be less than VBAT	1.8 V voltage domain, and be sure to
GPIO1	32	Ю	GPIO	In all usage states, the input voltage must be less than	follow the end specification
				VBAT	
Reserved	30		Pin empty connection		-
USIM interfa	ace				
Pin name	Pin number	I/O	Description	DC characteristics	Remarks



SIM_VDD	6	DO	USIM card power	V norm = 1.8 V	
SIM_RST	9	DO	USIM card reset signal	V <sub>OLmax</sub> = 0.25 × SIM_VDD	
SIM DATA	7	IO	USIM card data	V <sub>OHmin</sub> = 0.70 × SIM_VDD	
5 <i>_</i> 5,, .	,		signal	V <sub>ILmax</sub> = 0.20 × SIM_VDD	
				V <sub>IHmin</sub> = 0.75 × SIM_VDD	
				V <sub>OLmax</sub> = 0.25 × SIM_VDD	
				V <sub>OHmin</sub> = 0.70 × SIM_VDD	
SIM_CLK	8	DO	USIM card clock signal	V <sub>OLmax</sub> = 0.25 × SIM_VDD	
				V <sub>OHmin</sub> = 0.70 × SIM_VDD	
SIM_DET	10	DI	USIM card detection input		
		_			_
Antenna int	erface				
Antenna int	Pin number	I/O	Description	DC characteristics	Remarks
	Pin	I/O IO	Description  NB RF Antenna Interface	DC characteristics	50 Ω
Pin name	Pin number		NB RF Antenna	DC characteristics	50 Ω characteristic
Pin name	Pin number		NB RF Antenna	DC characteristics	50 Ω
Pin name  RF_ANT	Pin number 25	Ю	NB RF Antenna Interface BLE/Wi-Fi RF	DC characteristics	50 Ω characteristic
Pin name  RF_ANT  BT_ANT	Pin number 25	Ю	NB RF Antenna Interface BLE/Wi-Fi RF	DC characteristics  DC characteristics	50 Ω characteristic
Pin name  RF_ANT  BT_ANT  SPI interface	Pin number 25 27 e	10	NB RF Antenna Interface  BLE/Wi-Fi RF Antenna Interface		50 Ω characteristic impedance
Pin name  RF_ANT  BT_ANT  SPI interfact  Pin name	Pin number 25 27 e Pin number	10	NB RF Antenna Interface  BLE/Wi-Fi RF Antenna Interface  Description  Master input slave		50 Ω characteristic impedance  Remarks  1.8 V voltage
Pin name  RF_ANT  BT_ANT  SPI interfact  Pin name  SPI_MISO	Pin number 25  Pin number 17	IO IO DI	NB RF Antenna Interface  BLE/Wi-Fi RF Antenna Interface  Description  Master input slave output signal  Master output		50 Ω characteristic impedance  Remarks  1.8 V voltage



I2C interface	9	-			
Pin name	Pin number	I/O	Description	DC characteristics	Remarks
I2C_SCL	39	Ю	I2C clock signal		
I2C_SDA	40	Ю	I2C data signal		1.8 V voltage domain <sup>6</sup>

Table 4: Pin description

### 2.3. Operating modes

The following table briefly describes the three operating modes of the module.

Mode	Description
Active (connected)	The module is in the wake-up state; all functions are available normally, and data can be sent and received
Idle	The module is in pending state and can receive paging messages
PSM	The module is in a deep-sleep state, with only the RTC functioning internally and disconnected from the network

Table 5: Operating mode

### 2.4. Power saving mode (PSM)

The module consumes very low current in PSM (typical current consumption:  $2.5~\mu A$ ). The main purpose of PSM is to reduce the power consumption of the module and prolong the battery's power supply time. The figure below shows a schematic diagram of the module's power consumption in various modes.

<sup>&</sup>lt;sup>6</sup>1. The level of external peripherals must not exceed the range of 1.8 V ± 5% of the normal voltage domain, and it is forbidden to directly connect with peripherals outside the normal operating level range.

<sup>2.</sup> If peripherals with different voltages are used, be sure to use a level conversion circuit.

<sup>3.</sup> The internal I/Os of the module are connected in parallel to the same level. Once an I/O port has an incorrect level, it can lead to unpredictable issues during usage and operation of the module.



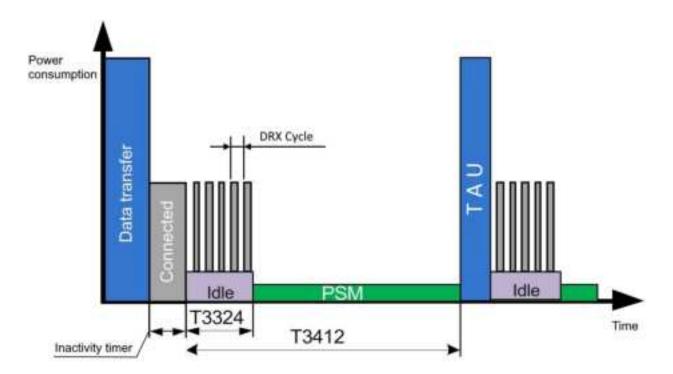


Figure 3: Power consumption diagram

The process for the module to enter PSM is as follows: Upon establishing a connection with the network or Tracking Area Update (TAU), the module will request to enter PSM in the request message, and the network will configure the T3324 timer value in the response message and return it to the module, thus initiating the reachable timer. When the T3324 timer expires, the module enters PSM. If the module is connected to the network or initializes the PDN (Public Data Network) for emergency services, it cannot apply to enter the PSM.

When the module is in PSM mode, all networking activities are closed. However, the T3412 timer, which is related to the periodic TAU update, is still functioning.

Any of the following methods can make the module exit PSM:

- When the T3412 timer expires, the module will automatically exit PSM.
- To wake up the module from PSM while it is in this mode, pull down either WAKE\_UP or CHIP\_ENB, as illustrated in the timing diagram below.



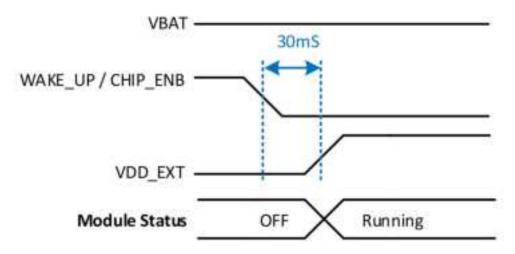


Figure 4: PSM wakeup sequence

### 2.5. Power supply design

Nimbus 220 has two VBAT pins for connecting an external power supply. The following table describes the module's VBAT pin and its ground pin.

Power supp	ly				
Pin name	Pin number	I/O	Description	DC characteristics	Remarks
VBAT	11, 12	PI	Module power supply	V max = 3.63 V V min = 2.97 V V norm = 3.3 V	
GND	13, 21, 23, 24, 26, 28	GND			

Table 6: Power pin

### 2.6. Power supply reference circuit

A module's power supply design is critical for its performance. Nimbus 220 can use an LDO with a low quiescent current and an output current capability of 1A as a power supply, and also supports Li-MnO2/2S battery power supply; its power input voltage range is 2.97 V to 3.63



V. When the module is operating in digital transmission, it must be ensured that the power supply does not drop below the minimum operating voltage of the module, which is 2.1 V, otherwise the module will malfunction.

In order to ensure better power supply performance, it is recommended to connect a low ESR (ESR = 0.7  $\Omega$ ) 100  $\mu$ F tantalum capacitor in parallel near the VBAT input of the module, as well as 100 nF, 100 pF (0402 package) and 22 pF (0402 package) filter capacitors. At the same time, it is recommended to add a TVS tube close to the VBAT input to improve the surge voltage withstand capability of the module. In principle, the longer the VBAT trace is, the wider the trace width should be. The reference circuit of the VBAT input terminal is shown in the figure below.

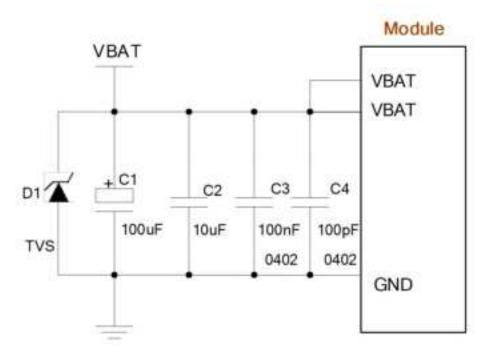


Figure 5: VBAT input reference circuit

#### 2.7. Power on/off

When the module is powered off, it can be powered on by pulling down CHIP\_ENB for a minimum of 500 ms.

Power butto	on interfac	е			
Pin name	Pin number	I/O	Description	DC characteristics	Remarks



PWRKEY 38 DI Pull down CHIP_ENB to power on the module	V <sub>IL</sub> max = 0.3 * VBAT V <sub>IH</sub> min = 0.7 * VBAT
--	--

Table 7: CHIP\_ENB pin

It is recommended to use an open-collector drive circuit to control the CHIP\_ENB pin. The reference circuit is as follows.

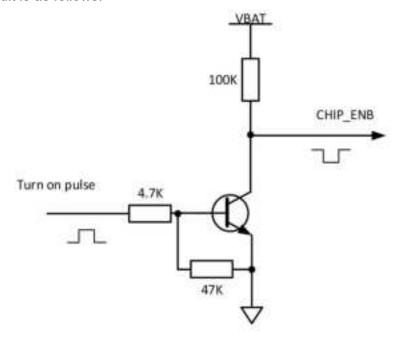


Figure 6: Open collector drive boot reference circuit

Another way to control CHIP\_ENB is directly through a push-button switch, with a transient voltage suppressor (TVS) tube placed near the button for electrostatic discharge (ESD) protection. The reference circuit is shown in the figure below.

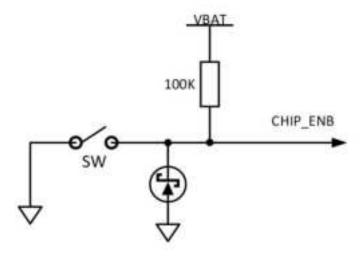




Figure 7: Button power-on reference circuit

The sequence diagram for module startup is as follows.

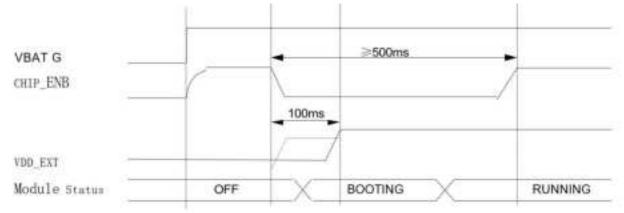


Figure 8: Boot sequence

The Nimbus 220 module can be shut down by any of the following methods:

- The module can be shut down by disconnecting the VBAT power supply;
- The module will automatically shut down when the power supply is less than 2.1 V.

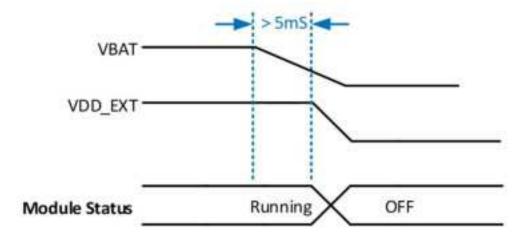


Figure 9: Shutdown sequence (disconnect VBAT shutdown)

#### 2.8. Reset module

The module can be reset by pulling down the RESET pin for at least 50ms.

**Reset interface** 



Pin name	Pin number	I/O	Description	DC characteristics	Remarks
RESET	34	DI	Reset		Active low

Table 8: Reset pin

The hardware reset reference circuit is shown in the figure below. It is recommended to use an open-collector drive circuit to control the RESET pin.

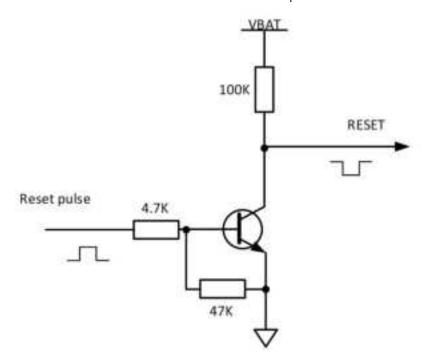


Figure 10: Open collector drive reference reset circuit

The RESET pin can also be controlled using a key.



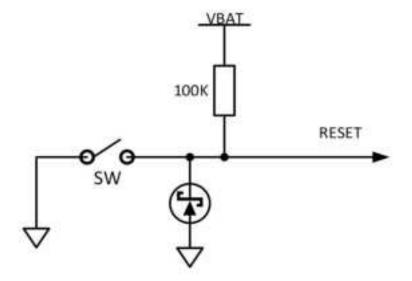


Figure 11: Button reset reference circuit

The reset timing diagram is as follows.

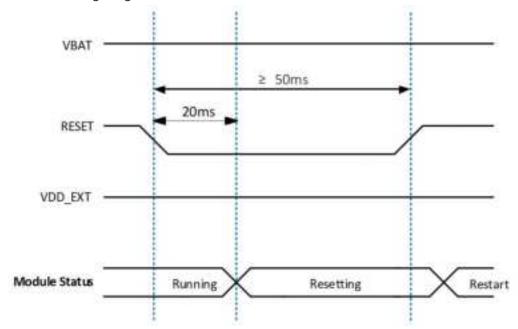


Figure 12: Reset timing

### 2.9. Wake up mode

When the module is in PSM mode, pull down WAKE\_UP for at least 30 ms to wake up the module.



WAKE_UP i	nterface	-			
Pin name	Pin number	I/O	Description	DC characteristics	Remarks
WAKE_UP	33	DI	External interrupt pin. Wake up from the PSM mode		Active low

Table 9: Wake up pin

The hardware reset reference circuit is shown in the figure below; it is recommended that an open-collector drive circuit be used to control the RESET pin.

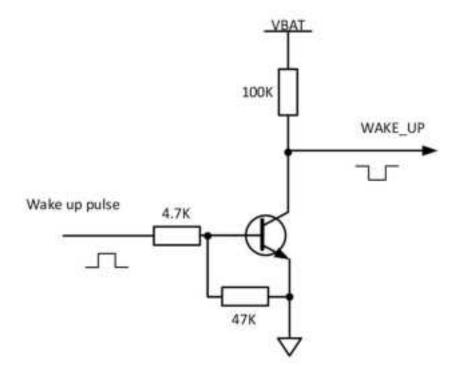


Figure 13: Open collector drive reference wake-up circuit

The RESET pin can also be controlled using a key.



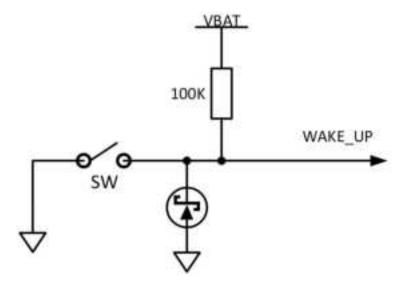


Figure 14: Key reference wake-up circuit

#### 2.10.Serial port

The module has three serial ports: main serial port, debugging serial port and auxiliary serial port. The module operates as DCE (Data Communication Equipment) and is connected in the traditional DCE-DTE (Data Terminal Equipment) way.

#### Main serial port:

- UART1\_TXD: Send data to the RXD end of the DTE device.
- UART1 RXD: Receive data from the TXD end of the DTE device.

#### Debug serial port:

- DBG TXD: Send data to the serial port of DTE.
- DBG RXD: Receive data from the serial port of DTE.

#### Auxiliary serial port:

- UART2 TXD: Send data to the serial port of DTE.
- UART2 RXD: Receive data from the serial port of DTE.

Interface	Pin name	Pin number	Description	Remarks
Main serial	UART1_RXD	3	Receive data	1.8 V voltage domain
F	UART1_TXD	4	Send data	
	UART1_RTS	2	Send data	



	UART1_CTS	1	Receive data	
Debug serial port	DBG_RXD	36	Receive data	1.8 V voltage domain
'	DBG_TXD	37	Send data	
Auxiliary serial port	UART2_RXD	18	Receive data	3.3 V voltage domain
	UART2_TXD	19	Send data	

Table 10: Serial port pin definition

The main serial port can be used for AT command transmission, data transmission and software upgrade.

After the module is turned on, it is in the adaptive serial transmission rate mode by default (the default is 115,200 bps serial transmission rate self-adjusting synchronization); the MCU needs to continuously send AT commands to the module for serial transmission rate synchronization, and if an "OK" is returned, it means the synchronization is successful; Following hibernation, the module will directly use the serial transmission rate that had been successfully synchronized after power-on, without needing to resynchronize.

The figure below shows a schematic diagram of the connection between a DCE and a DTE for the main serial port.

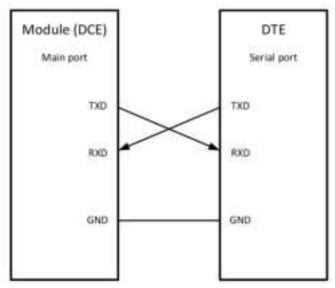


Figure 15: Schematic diagram of the main serial port's connection mode

With the debugging tool, customers can view the underlying log information through the debugging serial port for software debugging; its default serial transfer rate is 115,200 bps.

The figure below shows a schematic diagram of the connection between a DCE and a DTE for the debugging serial port.



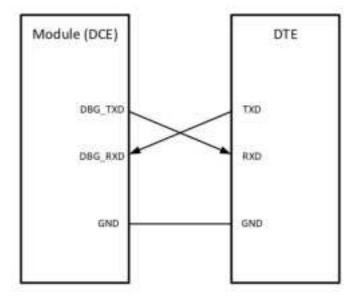


Figure 16: Schematic diagram of the debugging serial port's connection mode

With the debugging tool, customers can view the underlying log information through the auxiliary serial port for software debugging. Its default serial transfer rate is 115,200 bps. The schematic diagram of the connection between a DCE and a DTE is as follows.

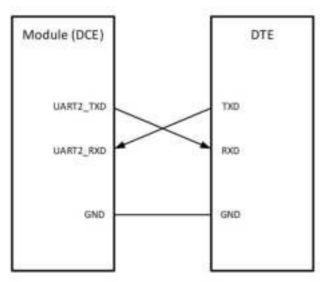


Figure 17: Schematic diagram of the auxiliary serial port's connection mode

The voltage domain of the serial port of this module is 1.8 V. If the voltage domain of the customer application system is 3.3 V, a level converter must be included in the serial connection between the module and the customer application system. The following figure provides a reference circuit design using a level conversion chip.



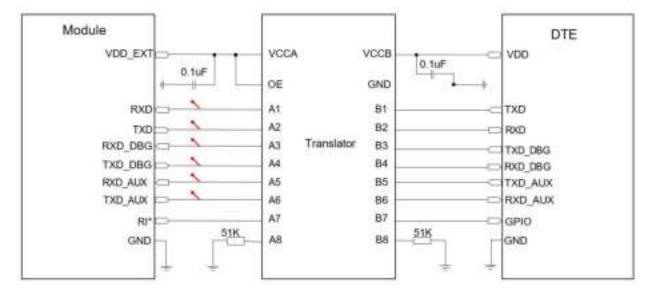
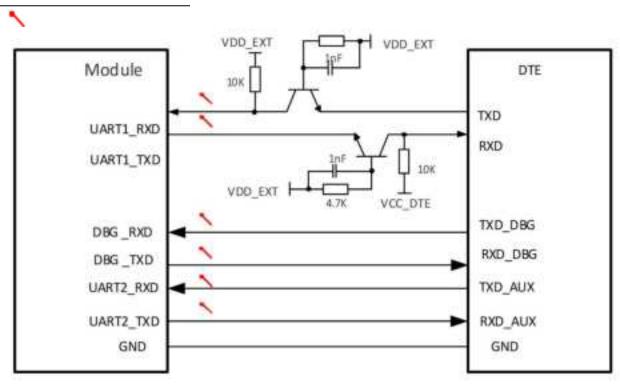


Figure 18: Level shifting reference circuit (level conversion chip)<sup>6</sup>

Another level shifting circuit is shown in the figure below. The input and output circuit design of the dotted-line part can be referred to the solid-line part, but attention should be paid to the connection direction.



<sup>&</sup>lt;sup>6</sup> Indicates the test point of the serial port. It is recommended to keep the test points of VBAT and PWRKEY to facilitate firmware upgrade and debugging when necessary.



Figure 19: Level shifting reference circuit (transistor)<sup>78</sup>

The figure below is a schematic diagram of the connection between the standard RS-232 interface and the module. Customers must ensure that the I/O voltage of the level conversion chip connected to the module is 1.8 V.

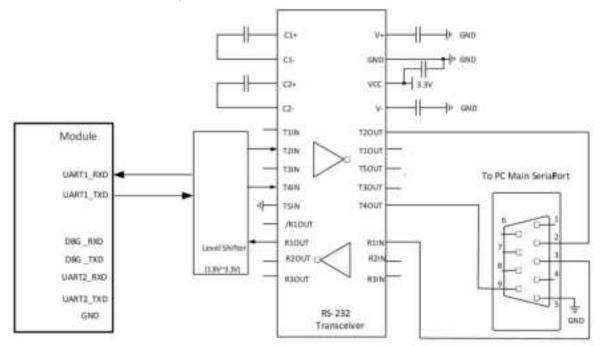


Figure 20: RS-232 interface diagram

#### 2.11.SPI interface

Nimbus 220 provides an SPI interface (the module acting as the host), and the following table lists the pin definitions of the SPI interface.

Pin name	Pin number	I/O	Description	Remarks
SPI_MISO	17	DI	Master input slave output signal	4.007
SPI_MOSI	16	DO	Master output slave input signal	1.8V voltage domain

<sup>&</sup>lt;sup>7</sup> Indicates the test point of the serial port. It is recommended to keep the test points of VBAT and PWRKEY to facilitate firmware upgrade and debugging when necessary.

<sup>8</sup> Transistor circuit solutions are not suitable for applications with serial transfer rates exceeding 460 Kbps.



SPI_SCLK	14	DO	Serial clock signal
SPI_CS	15	DO	Chip select signal

Table 11: SPI interface pin definition

The SPI interface voltage domain of this module is 1.8 V. If the system voltage domain of the slave device is 3.3 V, a level shifter needs to be added between the module and the slave device; it is recommended to use a level shifter that supports the SPI data rate. A reference circuit is shown in the figure below.

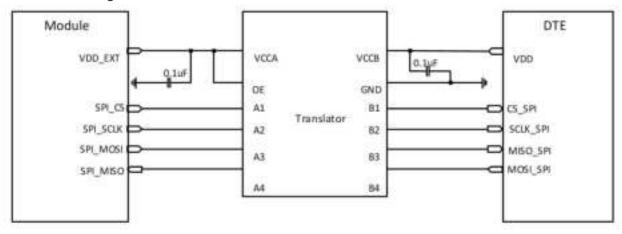


Figure 21: SPI interface level shifting reference circuit

#### 2.12.USIM interface

The USIM interface of the Nimbus 220 module complies with the ISO/IEC 7816-3 specification and supports 1.8 V / 3.0 V external USIM cards, powered by the power supply inside the module.

Pin name	Pin number	Description	Remarks
SIM_VDD	6	USIM card power	Voltage accuracy: 1.8 V / 3.0 V ± 5 % Maximum supply current: about 60 mA
SIM_RST	9	USIM card reset signal	
SIM_DATA	7	USIM card data signal	



SIM_CLK	8	USIM card clock signal	
SIM_DET	10	USIM card detection input	

Table 12: USIM interface pin definition

The figure below is the reference design of the 7-pin external USIM card holder.

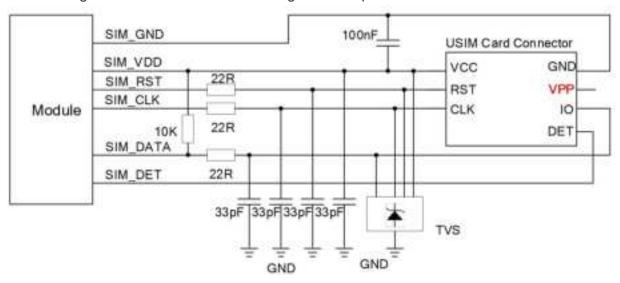


Figure 22: 7-pin external USIM card holder reference circuit diagram

In the circuit design of the USIM interface, it is recommended to follow the design principles described below in order to ensure good performance of the external USIM card and prevent it from being damaged.

- The external USIM card holder should be placed close to the module, and the length of the signal cable should not exceed 200 mm to ensure optimal performance.
- The external USIM card socket signal cable should be routed away from both the RF trace and the VBAT power cable.
- The ground of the external USIM card socket and the SIM\_GND wiring of the module should be short and thick, ensuring a wiring width of not less than 0.5 mm to ensure the same potential. The decoupling capacitor of SIM\_VDD should not exceed 1 uF, and should be placed close to the external USIM card socket.
- To prevent interference between the SIM\_CLK and SIM\_DATA signals, their wiring should not be too close, and a ground shield should be placed between them. Furthermore, the SIM\_RST signal should also be provided with a ground shield.
- To ensure optimal ESD protection performance, it is recommended to add a TVS tube to the pin of the external USIM card holder, where the parasitic capacitance should not



exceed 50 pF. The ESD protection device should be placed as close as possible to the external USIM card socket, and the signal routing should run from the socket to the device, then to the module. A 22-ohm resistor should be connected in series between the module and the external USIM card to suppress stray EMI and bolster ESD protection. To further improve performance, peripheral components of the external USIM card should be placed as close as possible to the external USIM card holder.

 Connect 33 pF capacitors in parallel to the SIM\_DATA, SIM\_VDD, SIM\_CLK, and

SIM RST lines to filter out radio-frequency interference.

### 2.13.ADC interface

The module provides a 10-bit analog-to-digital conversion input interface to measure the voltage value. The A/D interface operates in both Active and Idle modes.

Pin name	Pin number	Description
ADC	29	Universal analog-to-digital conversion interface

Table 13: ADC interface pin definition

The following is the ADC peripheral reference design circuit. The detection voltage is connected either in series with 0  $\Omega$  or directly to the ADC pin, with a filter capacitor connected in parallel near the module.

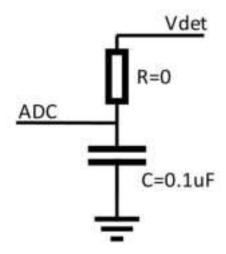


Figure 23: ADC peripheral reference circuit9

<sup>&</sup>lt;sup>9</sup> Ensure that Vdet does not exceed 5V, including possible spikes during power on and off and use, as this could result in IC damage.



### 2.14. Network status indicator

The NETLIGHT signal can be used to indicate the network status of the module. The connection reference circuit of the network status indicator is shown in the figure below.

Pin name	Pin number	I/O	Description
NETLIGHT	35	DO	Network status indicator

Table 14: NETLIGHT pin definition

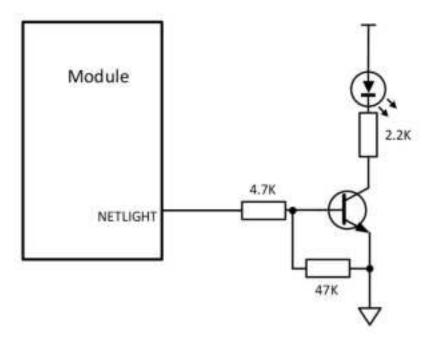


Figure 24: Network status indication reference circuit

### 3. Antenna interface

Pin 35 is the RF antenna interface of the module. The impedance of the RF antenna port is 50  $\Omega$ .

### 3.1. Pin definition

Pin name	Pin number	Description
RF_ANT	25	NBRF Antenna Interface
GND	22, 22, 23, 24, 26, 28	Ground

Table 15: RF antenna pin definition



### 3.2. Operating frequency

Frequency band	Receiving frequency	Transmit frequency
B13	746 MHz – 756 MHz	777 MHz – 787 MHz
B103	757 MHz – 758 MHz	787 MHz – 788 MHz

Table 16: Module operating frequency

#### 3.3. RF antenna reference circuit

It is recommended to reserve a  $\pi$ -type matching circuit in the peripheral circuit design of the antenna interface in order to better adjust the radio frequency performance. The components of the  $\pi$ -type matching circuit should be placed as close to the antenna as possible and selected according to the actual situation. By default, C1 and C2 are omitted and only a 0 ohm resistor is attached to R1.

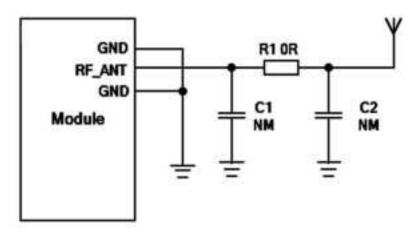


Figure 25: RF antenna reference circuit

The Nimbus 220 module provides an RF pad interface for connecting an external antenna, with ground pads on either side for improved grounding performance.

### 3.4. RF signal cable layout reference guide

For the user PCB, the characteristic impedance of all RF signal lines should be controlled to  $50~\Omega$ . In general, the impedance of an RF signal line is determined by the dielectric constant of the material, the trace width (W), the ground clearance (S), and the height of the reference ground plane (H). The control of PCB characteristic impedance is usually accomplished through two methods: microstrip line and coplanar waveguide. To illustrate the design principle, the following



figures show the structural design of the microstrip line and the coplanar waveguide when the impedance line is controlled to  $50~\Omega$ .

• The complete structure of the microstrip line.

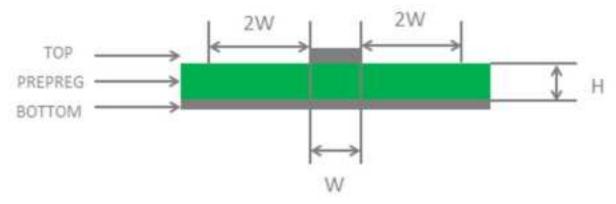


Figure 26: Two-layer PCB board microstrip line structure •

Complete structure of coplanar waveguide.

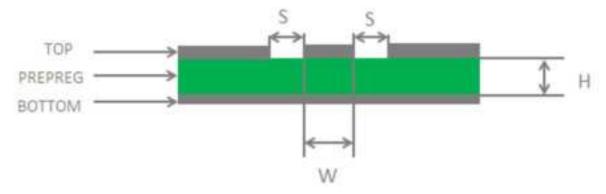


Figure 27: Two-layer PCB coplanar waveguide structure



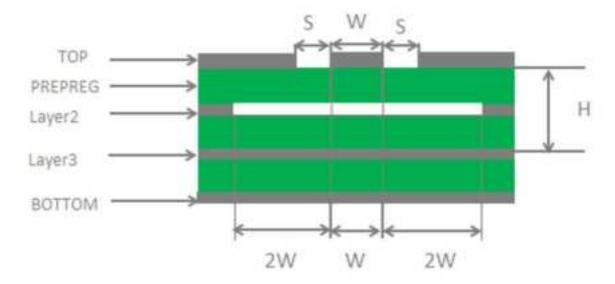


Figure 28: Four-layer PCB coplanar waveguide structure (the reference ground is the third layer)

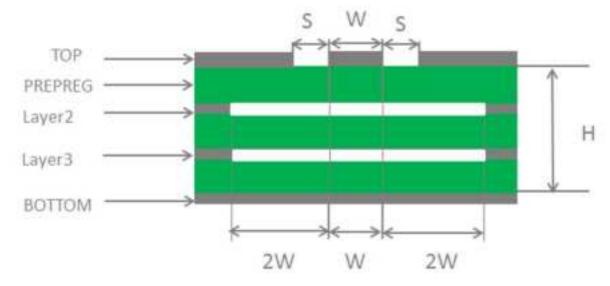


Figure 29: Four-layer PCB coplanar waveguide structure (the reference ground is the fourth layer)

To ensure good performance and reliability of the RF signal in the circuit design of the RF antenna interface, the following design principles are recommended:

- The impedance simulation calculation tool should be used to precisely control the  $50\Omega$  impedance on the RF signal line.
- The GND pin adjacent to the RF pin should not be used as a thermal pad, but should be fully in contact with the ground plane.



- The distance between the RF pin and the RF connector should be kept as short as possible; additionally, right-angle routing should be avoided, with a recommended routing angle of 135 degrees.
- Care should be taken when constructing the package of the connecting device, and a certain distance should be maintained between the signal pin and the ground.
- The reference ground plane of the RF signal line should be complete; adding a certain number of ground holes around the signal line and the reference ground can improve the RF performance; the distance between the ground hole and the signal line should be at least twice the line width (2\*W).

#### 3.5. Antenna requirements

The table below lists the requirements for NB-IoT antennas.

Frequency band	Loss
LTE B13/103	Insertion loss: <1dB

Table 17: Antenna insertion loss requirements

Parameter	Requirement
Frequency	LTE B13/103
VSWR	≤ 2
Efficiency	> 30%
Maximum input power (W)	50
Input Impedance (Ω)	50

Table 18: Antenna parameter requirements

### 3.6. RF output power

Frequency band	Maximum value	Minimum value	
B13	23 dBm ± 2 dB	< -39dBm	
B103	23dBm ± 2 dB	< -39dBm	

Table 19: RF conducted power<sup>11</sup>



### 3.7. RF receive sensitivity

Frequency	Conducted reception sensitivity
B13	-129 dBm
B103	-129 dBm

Table 20: RF retransmission sensitivity

# 4. Electrical performance and reliability

### 4.1. Operating and storage temperature

The table below shows the module operating and storage temperature range.

Parameter	Minimum value	Typical value	Maximum value	Unit
Normal operating temperature <sup>12</sup>	-25	+25	+75	°C
Extended operating temperature <sup>13</sup>	-30		+85	°C
Storage temperature	-40		+90	°C

Table 21: Operating and storage temperature range

<sup>&</sup>lt;sup>11</sup> The design complies with the NB-IoT protocol in 3GPP Rel.13 and 3GPP Rel.14.

<sup>&</sup>lt;sup>12</sup> When the module works in this temperature range, the relevant performance of the module meets the requirements of the 3GPP standard.

<sup>&</sup>lt;sup>13</sup> When the module works within this temperature range, it can still maintain a normal working state, with functions such as SMS and data transmission, and there will be no irreparable faults; the radio frequency spectrum and network are largely unaffected. However, the values of individual indicators such as output power may exceed the scope of 3GPP standards. When the temperature returns to the normal operating temperature range, the indicators of the module will still meet the 3GPP standard.



### 4.2. Power consumption

The current consumption values are shown in the table below. The measured values in the table are for reference only. For more accurate and detailed test reports, please find them in the relevant materials of the power consumption test.

Parameter	Mode	Description	Minim um value	Typical value	Maxim um value	Unit
Ivbat	PSM	Sleep state		2.3		μA
	Idle	@eDRX=81.92s, PTW=40.96s		45		μА
		@DRX=1.28s		541		μΑ
		@DRX=2.56s		800		μΑ
		B5 @0Bm, instrumented test		35		mA
		B8 @0dBm, instrument test		36		mA
		B5 @23dBm, instrument test		307		mA
		B8 @23dBm, instrument test		329		mA

Table 22: Module power consumption

#### 4.3. Static Protection

Due to the static electricity generated by the human body and the charged friction between microelectronics, static electricity may be discharged to the module through various channels in the application process, causing certain damage to the module. Thus, ESD protection should be paid attention to throughout the research and development, production assembly and testing, especially during product design. Anti-static protection should be added at the interface of circuit design and points that are susceptible to damage or influence by electrostatic discharge; additionally, anti-static gloves should be worn during production. Friction between microelectronics, static electricity can be discharged to the module through various channels, which may cause certain damage, thus emphasizing the need for ESD protection. During the process of research and development, production assembly, and testing, especially in product



design, ESD protection measures should be taken. For example, anti-static protection should be added to the interface of circuit design and points that are susceptible to damage or influence by electrostatic discharge; furthermore, anti-static gloves should be worn during production.

The following table shows the ESD withstand voltage of the module pins.

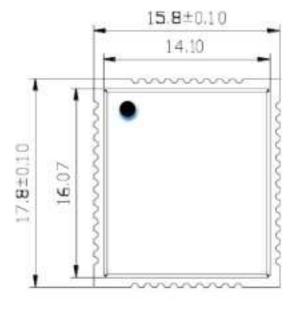
Test point	Contact discharge	Air discharge	Unit
VBAT, GND	±5	±10	kV
Antenna interface	±5	±10	kV
Other interfaces	±0.5	±1	kV

Table 23: ESD Performance Parameters (Temperature: 25 °C, Humidity: 45 %)

### 5. Mechanical Dimensions

This chapter describes the mechanical dimensions of the module, all of which are in millimeters. For those dimensions without specified tolerances, the tolerance is  $\pm 0.05$ mm.

#### 5.1. Module mechanical size



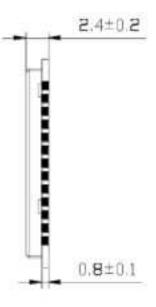


Figure 30: Top and side dimension drawing (unit: mm)



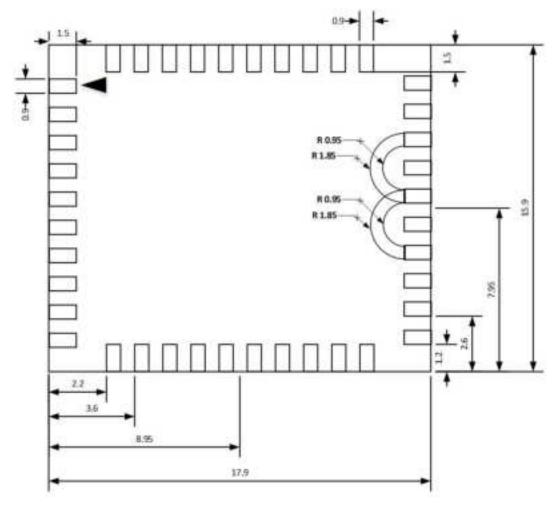


Figure 31: Module bottom view dimensions (bottom view)



### 5.2. Recommended package

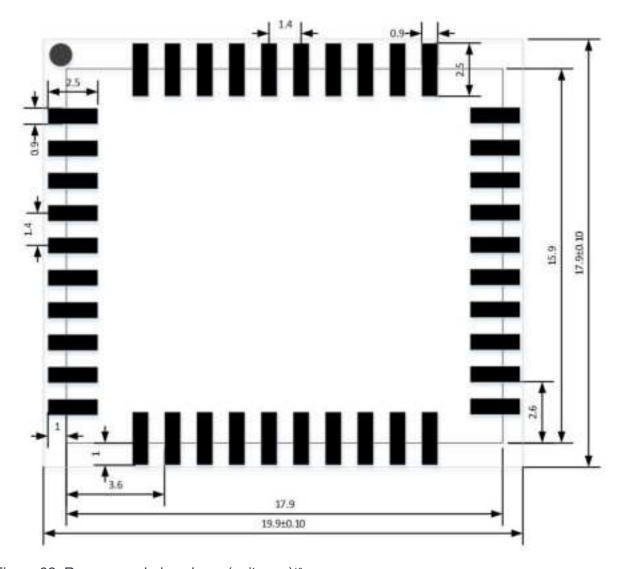


Figure 32: Recommended package (unit: mm)<sup>10</sup>

<sup>&</sup>lt;sup>10</sup> In order to ensure that the module can be installed normally, a distance of at least 3 mm should be kept between the module and other components on the PCB.



# 5.3. Module top view / bottom view



Figure 33: Module top view<sup>11</sup>

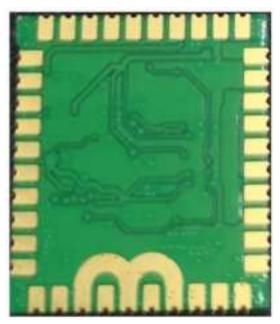


Figure 34: Module Bottom View

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<sup>&</sup>lt;sup>11</sup> It is the design rendering of the Nimbus 220 module



### 6. FCC Statement

FCC Statement This device complies with part 15 of the FCC Rules. Operation is subject to the following two conditions:

- 1. This device may not cause harmful interference, and
- 2.this device must accept any interference received, including interference that may cause undesired operation.

FCC Caution: Any changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate this equipment.

This transmitter must not be co-located or operating in conjunction with any other antenna or transmitter.

#### **6.2.1. Radiation Exposure Statement**

This equipment complies with FCC radiation exposure limits set forth for an uncontrolled environment. This equipment should be installed and operated with minimum distance 28 cm between the radiator and your body.

This device is intended only for OEM integrators under the following conditions:

- 1. The antenna must be installed such that 28 cm is maintained between the antenna and users, and
- 2. The transmitter module may not be co-located with any other transmitter or antenna. 41111094 Rev 1.7 August 10, 2018 52 Product Technical Specification Legal Information As long as the 2 conditions above are met, further transmitter test will not be required. However, the OEM integrator is still responsible for testing their end-product for any additional compliance requirements required with this module installed.

**IMPORTANT NOTE**: In the event that these conditions cannot be met (for example certain laptop configurations or co-location with another transmitter), then the FCC authorization is no longer considered valid and the FCC ID cannot be used on the final product. In these circumstances, the OEM integrator will be responsible for re-evaluating the end product (including the transmitter) and obtaining a separate FCC authorization.

#### 6.2.2. End Product Labeling

This transmitter module is authorized only for use in device where the antenna may be installed such that 20 cm may be maintained between the antenna and users. The final end product must be labeled in a visible area with the following: "Contains FCC ID:2AXTDEDMXNLTEG". The grantee's FCC ID can be used only when all FCC compliance requirements are met.

#### 6.2.3. Manual Information to the End User

The OEM integrator has to be aware not to provide information to the end user regarding how to install or remove this RF module in the user's manual of the end product which integrates this module. The end user manual shall include all required regulatory information/warning as show in this manual.

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# Appendix A Terminology abbreviations

Abbreviation	Description	
ADC	Analog-to-Digital Converter	
CoAP	Constrained Application Protocol	
DCE	Data Communications Equipment (typically module)	
DTE	Data Terminal Equipment (typically computer, external controller)	
DTLS	Datagram Transport Layer Security	
ЕМІ	Electromagnetic Interference	
ESD	Electrostatic Discharge	
FTP	File Transfer Protocol	
HD-FDD	Half-Duplex Frequency Division Duplexing	
НТТР	Hyper Text Transfer Protocol	
HTTPS	Hyper Text Transfer Protocol over Secure Socket Layer	
I/O	Input/Output	
kbps	Kilo Bits Per Second	
LED	Light Emitting Diode	
Li-MnO2	Lithium-manganese Dioxide	
Li-2S	Lithium Sulfur	
LTE	Long Term Evolution	
LwM2M	Lightweight M2M	



MQTT	Message Queuing Telemetry Transport	
NB-IoT	Narrow Band- Internet of Things	
PCB	Printed Circuit Board	
PDU	Protocol Data Unit	
PPP	Point-to-Point Protocol	
PSM	Power Saving Mode	
RF	Radio Frequency	

Abbreviation	Description	
RTC	Real Time Clock	
RXD	Receive Data	
SMS	Short Message Service	
SSL	Secure Sockets Layer	
ТСР	Transmission Control Protocol	
TE	Terminal Equipment	
TXD	Transmitting Data	
UART	Universal Asynchronous Receiver & Transmitter	
UDP	User Datagram Protocol	
URC	Unsolicited Result Code	
USIM	(Universal) Subscriber Identification Module	
VSWR	Voltage Standing Wave Ratio	

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V max	Maximum Voltage Value	
V norm	Normal Voltage Value	
V min	Minimum Voltage Value	
V⊪max	Maximum Input High Level Voltage Value	
V <sub>IH</sub> min	Minimum Input High Level Voltage Value	
V <sub>IL</sub> max	Maximum Input Low Level Voltage Value	
V <sub>IL</sub> min	Minimum Input Low Level Voltage Value	
V₁max	Absolute Maximum Input Voltage Value	
V <sub>I</sub> norm	Absolute Normal Input Voltage Value	
V <sub>I</sub> min	Absolute Minimum Input Voltage Value	
V <sub>OH</sub> max	Maximum Output High Level Voltage Value	
V <sub>OH</sub> min	Minimum Output High Level Voltage Value	
V <sub>OL</sub> max	Maximum Output Low Level Voltage Value	
V <sub>OL</sub> min	Minimum Output Low Level Voltage Value	

# Revision history

Revision	Date	Description
1.0	August 2023	Initial release

## Contact

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