Thundercomm TurboX™ C865 System on Module

A high performance embedded platform based on Qualcomm® Snapdragon™ QRB5165 processor

Description

Thundercomm TurboX™ C865 System on Module (SOM) is a high performance intelligent module, integrating Android, based on Qualcomm QRB5165 processor. It integrates the advanced 7 nm Fin FET process, a customized 64-bit Octa-core Qualcomm Kryo 585 applications processor.

C865 SOM supports long range Wi-Fi, Wi-Fi 6 (Wi-Fi 802.11 a/b/g/n/ac/ax) and BT5.1. It supports one 5040 x 2160@60Hz or two 2560 x2560@120fps display, support up to 12 cameras with 7 concurrent, integrates multiple audio and video input/output interfaces. It provides a variety of GPIO, I2C, UART and SPI standard interfaces. In addition, it supports two 4-lane MIPI-DSI, six 4-laneMIPI-CSI together with SOM common standard protocol interfaces such as USB3.1, PCIE2.1/3.0 and I2S.

C865 SOM provides convenient and stable system solution for IOT field, it can be embedded into the device on VR/AR, Robot, Smart Camera, AI devices, and any other connecting fields. The size of module is 56mm x 45mm x 9.06mm, besides a 500pins B2B connector.

Features

The following table shows the detailed features of QRB5165 and C865 SOM.

QRB5165	
Applications Processor	Kryo 585-64-bit applications processor with a 4MB L3 cache ■Quad high-performance Kryo Gold cores ■Quad low-power Kryo Silver cores
Digital signal processing	■Compute Hexagon DSP with quad Hexagon Vector eXtensions (quad-HVX) and Hexagon Co-processor (Hexagon CP) 2.0 ■Audio Hexagon DSP dedicated to audio subsystem ■Sensor Hexagon DSP in the Qualcomm All-Ways Aware Hub to support always-on, low-power use cases ■All Hexagon DSP are cache-based processors with full access to DDR

Graphics	■Adreno GPU 650 - 4K 60 fps UI or 2x 2k 60 fps UI ■OpenGL ES 3.2, Vulkan 1.1, DX12 FL 12_1 ■OpenCL 2.0 full profile
Display support	2 x 4-lane DSI D-PHY 1.2 and DisplayPort 1.4 data concurrency over USB Maximum concurrency configurations ■5040 × 2160 at 60 Hz 30bpp primary + 3840 × 2160 at 60 Hz 30bpp DisplayPort or 3840 × 2160 at 60 Hz 30bpp Wi-Fi display ■5040 × 2160 at 60Hz 30bpp primary + 7680 × 4320 at 30 Hz 24bpp DisplayPort ■5040 × 2160 at 60Hz 30bpp primary + 2 × 3840 ×2160 at 60 Hz DisplayPort
Video Encode	4K120/8K30 encode for H.265 Main 10, H.265 Main, H.264 High, and VP8 codecs
Video Decode	4K240/8k30 decode for H.265 Main 10, H.265 Main, H.264 High, VP9 profile 2, VP8, and MPEG-2 codecs
Camera support	■Qualcomm Spectra 480 Camera ISP ■Support 6 x 4 Lane MIPI CSI ■Real-time sensor input resolution: 25 + 25 + 2 + 2 + 2 + 2 + 2 MP ■64 MP 30 fps ZSL with a dual ISP
WLAN	2.4G/5G, support 802.11 a/b/g/n/ac/ax, 2 x 2 MIMO
Bluetooth	■Support Bluetooth 5.1 + HS ■BLE
ADC Interface	■Support ADC interfaces ■Used for input voltage sense, battery temperature detection and general purpose ADC

C865 SOM	
Processor	Snapdragon™ QRB5165
Memory	LPDDR5(POP) + UFS3.1, 8GB + 128GB
Connectivity	WiFi /BT: QCA6391 (2x2 MIMO, 802.11 a/b/g/n/ac/ax & BT5.1)
Display Interfaces	2 x MIPI-DSI 4-lane, 5040 x 2160@60fps
Camera Interfaces	6x 4 data lane MIPI CSI

Audio Interface	■SoundWire interface for codec ■SoundWire interface for smart speaker amplifier ■3x MI2S with two data lanes to support full duplex stereo ■1x MI2S with four data lanes for up to eight channels ■3 DMIC ports supports up to 6 DMICs
USB	2x USB 3.1 GEN2, one can support Type-C with DisplayPort
PCIe	2 x 2-lane PCIe Gen3.0
Other Interfaces	■2 x RF connector for WiFi /BT, 2 x USB 3.1, 2 x PCIE, 1 x UART, 1 x SDC for SD card, 6 x DMICs, 2 x Speakers ■11 x 4pin QUPs(can be set as 4pin SPI or 2pin I2C) ■2 x QUPs can be set as 2pin I2C ■4 x camera dedicated I2Cs ■2 x sensor dedicated I2Cs ■1 x sensor dedicated SPI
Operating Environment	■Operation Temperature: --20℃ ~ 70℃ ■Operation Humidity: 5%~95%, non-condensing
Power supply	3.8V ~ 4.2V
Dimension	45 x 56 x 9mm w/B2B Connector
RoHS	All hardware components are fully compliant with EU RoHS 2.0 directive

Applications

TurboX C865 SOM is ideal for many applications including (but not limited to): AI, Robotics, Virtual Reality (VR), Augmented Reality (AR), Drones and Medical Devices.

Revision History:

Version	Date	Description
V1.0	May.30, 2020	Revised Release
V1.1	Jan 05, 2021	1. Add notes for alt functions of pin D38 E37 K41 K42

		2. Change GPIO 117 to GPIO 70
V1.2	Jan 21,2021	Fix typo for pin number of CCI_I2C in chapter 2.2.4
V1.3	Apr.16, 2021	Fix typo for pin number of table2.2-1 for VREG_IO_1P8, from B44 to B43; Fix typo for pin number of table2.2-8 for SD_UFS_CARD_DET_N, from G34 to G43

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1 Physical Description

1.1 Hardware Block Diagram

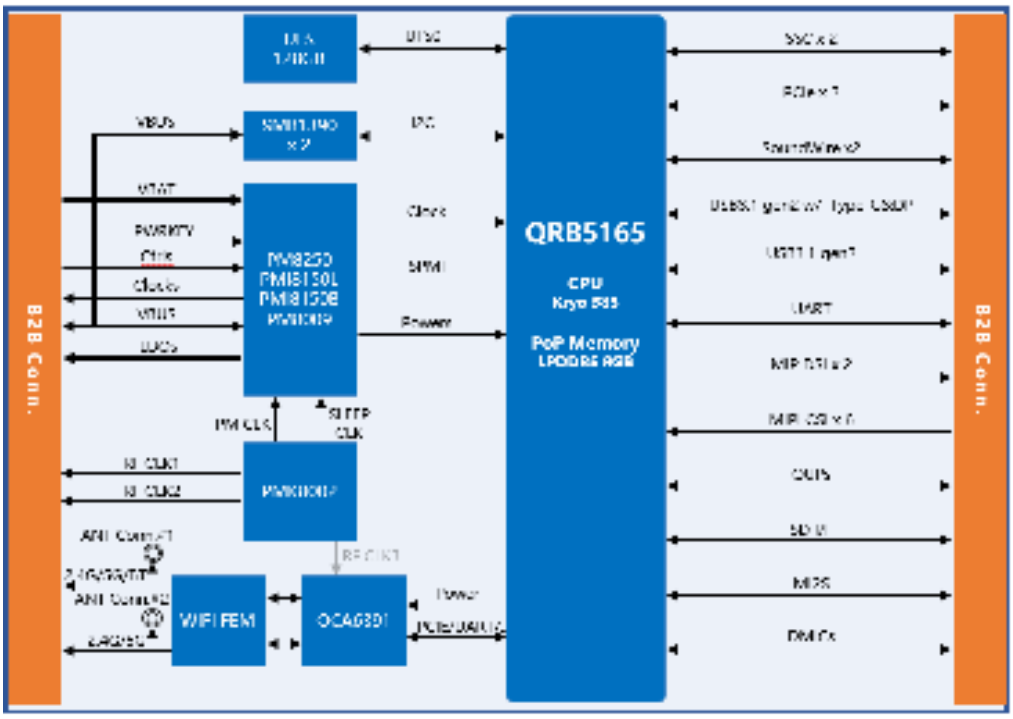

Figure 1.1-1 TurboX C865 SOM Hardware System Block Diagram

1.2 Major Components Location

TurboX C865 SOM's major components as below map.

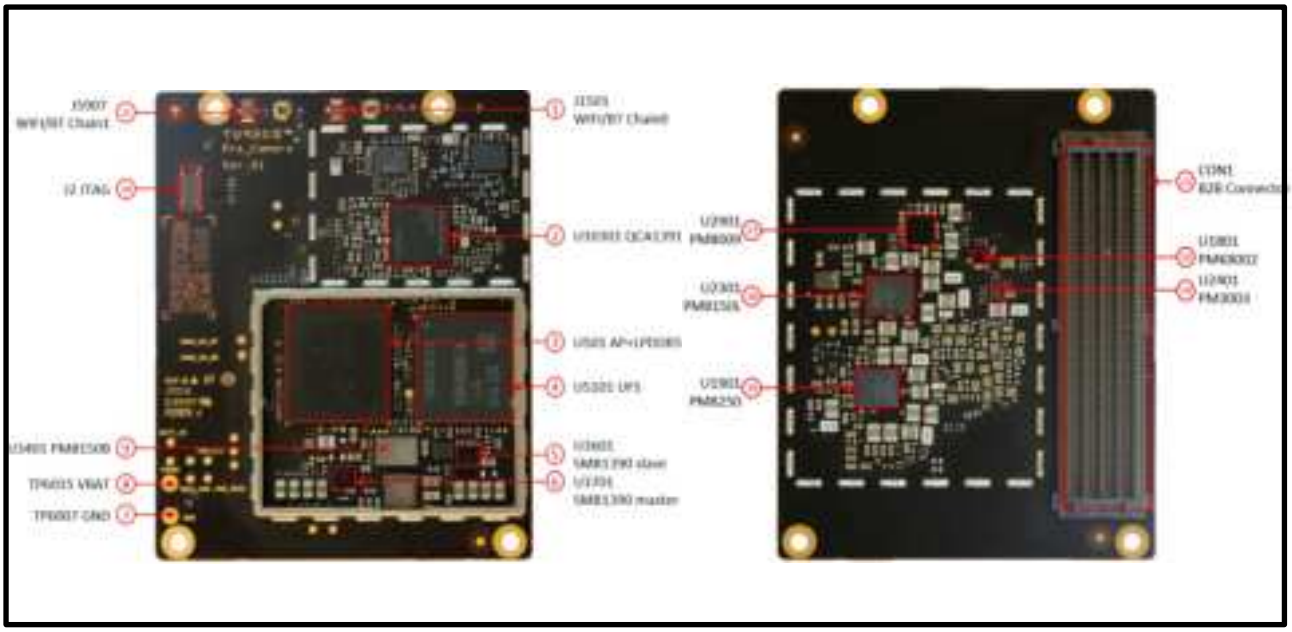

Figure 1.2-1 TurboX C865 SOM Key component Location

1.3 Connectors Function and Part Number

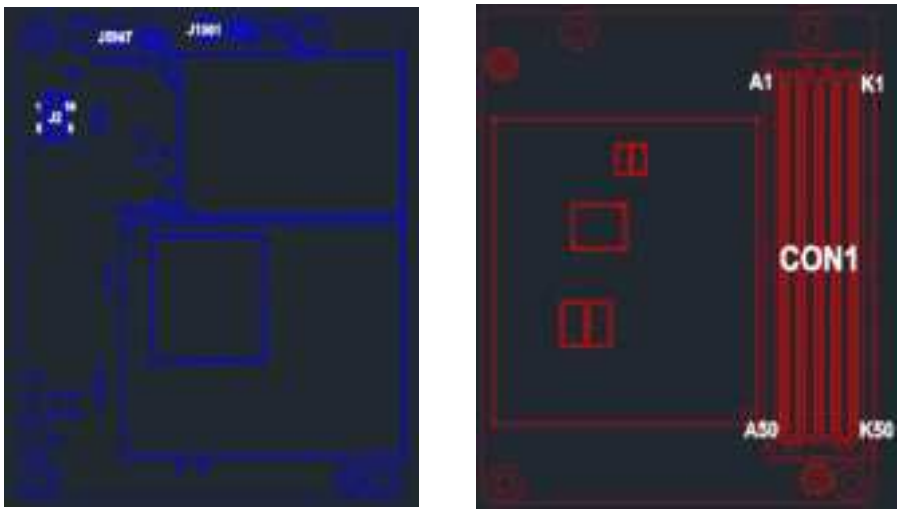

Figure 1.3-1 TurboX C865 SOM Connector PIN Location

Below table indicates connectors detail information.

Part Reference	Description	Manufacturer Part Number	Manufacturer

CON1	BTB connectors, used for connecting to Carrier Board.	SEAM8-50-S02.0-L-10-2	SAMTEC
J2	JTAG connector, used for JTAG Debug	AXF5D1612	Panasonic
Or J2	JTAG connector, used for JTAG Debug	20843-050E-21	I-PLEX
J1501,J5907	RF antenna connector	20449-001E	I-PLEX

Table 1.3-1 Connector part number and information

1.4 Package Drawing and Dimensions

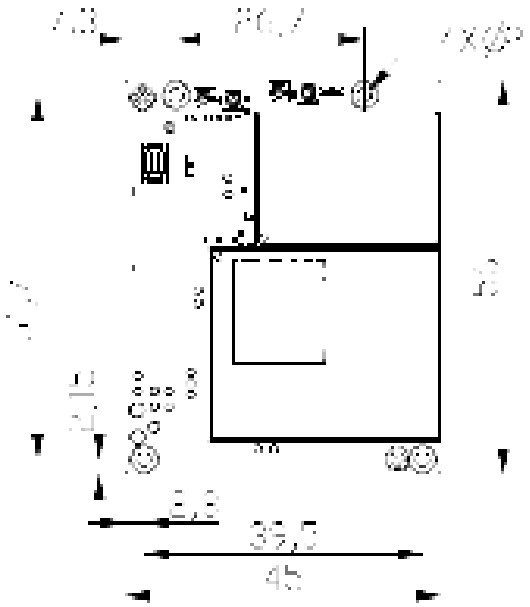

Figure 1.4-1 Top View

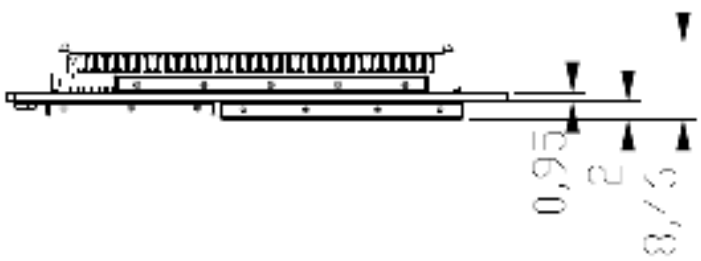

Figure 1.4-2 Side View

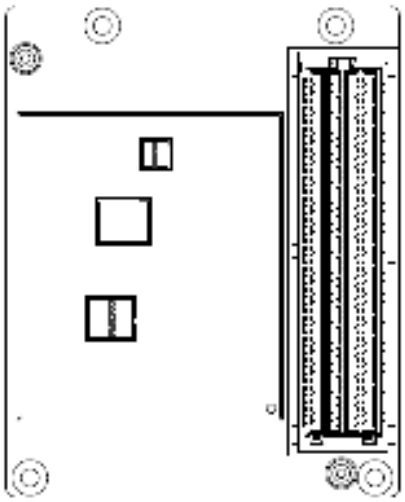

Figure 1.4-3 Bottom View

2 Interfaces Description

This chapter introduces all the interfaces definition, purpose to guide developer easy to design and verification on Thundercomm TurboX™ C865 SOM.

2.1 Interfaces Parameter Definitions

Symbol	Description
AI	Analog input
AO	Analog output
B	Bidirectional digital with CMOS input
CSI	Supply voltage for MIPI_CSI circuits and I/O; (1.2 V for low power mode)
DI	Digital input(CMOS)
DSI	Supply voltage for MIPI_CSI circuits and I/O; (1.2 V for low power mode)
DO	Digital output(CMOS)
H	High-voltage tolerant
nppdpukp	Programmable pull resistor. The default pull direction is indicated using capital letters and is a prefix to other programmable options: NP: pdpukp = default no-pull with programmable options following the colon (:) □ PD: nppukp = default pull-down with programmable options following the colon (:) PU: nppdkp = default pull-up with programmable options following the colon (:) □ KP: nppdpu = default keeper with programmable options following the colon (:)
KP	Contains an internal weak keeper device (keepers cannot drive external buses)
MIPI	Mobile industry processor interface
NP	Contains no internal pull
OD	Open drain
PD	Contains an internal pull-down device
PI	Power input
PO	Power output

PD	Contains an internal pull-down device
PU	Contains an internal pull-up device
P3	Power group 3, it is 1.8V.
P2	SDC Power group 2, it is 1.8V or 2.95V.

Table 2.1-1 Interfaces parameter definitions

2.2 Interfaces Detail Description

2.2.1 Power Supply Interface

Below table describes all interfaces of SOM Power Supply. For the detail parameter request, please refer the chapter on Electrical specifications.

Power Supply					
PIN Name	**Conn.**	**PIN**	**Type**	**Description, V_typ@I_rated**	**Note**
VBAT_CON	CON1	J47,J48,J49,J50,K47,K48,K49,K50	PI	Power supply input for SOM	
USB_VBUS	CON1	E47,E48,E49,E50	PO	USB output during USB-OTG operation.	
VREG_L11C_3P3	CON1	A49	PO	LDO, 3.1V@600mA	
VREG_L9C_2P96	CON1	A50	PO	LDO, 2.96V@600mA	
VREG_L5C_1P8	CON1	B4, B5	PO	LDO, 1.8V@150mA	
VREG_L8C_1P8	CON1	B42	PO	LDO, 1.8V@150mA	
VREG_IO_1P8	CON1	B43	PO	VREG SPMI output for SPMI PAD and PX0	
VREG_L2A_3P1	CON1	D43	PO	LDO, 3.1V@150mA	
VREG_S4A_1P8	CON1	D45, D46	PO	BUCK, 1.8V@3500mA	
VREG_BOB	CON1	D47, D48	PO	Buck-boost output, 3.3V	
VPH_PWR	CON1	D49, D50	PO	Primary system supply node	
GND	CON1	A1,A3,A5,A12,A14,A16,A18,A20,A22,A24,A26,A28,A30,A32,A34,A36,B2,B3,B48,B49,B50,C1,C3,C11,C13,C15,C17,C19,C21,C23,C25,C27,C29,C31,C33,C35,C4,C48,C49,C50,D2,D4,D12,D14,D16,D18,D20,D22,	GND	GND	

		D24,D26,D28,D30,D32,D34,E3,F11,F13,F15,F17,F19,F21,F23,F25,F27,F29,F31,F33,F35,F47,F48,F49,F50,G11,G13,G15,G17,G19,G21,G23,G25,G27,G48,G49,G50,H12,H14,H16,H18,H20,H22,H24,H48,H49,H50,K11,K13,K15,K17,K19,K21,K23,K25			

Table 2.2-1 Power Supply Definition

2.2.2 Touchscreen Interface

Touchscreen panels are supported using I2C buses and GPIOs configured as discrete digital inputs.

Touchscreen						
PIN Name	**Location**	**PIN**	**Voltage**	**Type**	**Description**	**Notes**
TS_I2C_SDA	CON1	E42	P3	OD	QUP13 I2C signals	
TP_I2C_SCL	CON1	D41	P3	OD	QUP13 I2C signals	
TP_INT_N	CON1	D40	P3	DO	TP interrupt signals	
TP_RESET_N	CON1	D42	P3	DI	TP reset signals	

Table 2.2-2 Touchscreen interfaces definition

2.2.3 Display Interface

The SOM supports dual 4-lane MIPI_DSI interfaces. 60fps, 5040 x 2160.

Display						
PIN Name	**Location**	**PIN**	**Voltage**	**Type**	**Description**	**Notes**
DSI0_A0_LN0_P	CON1	K16	DSI	AO	MIPI0 signals for MIPI LCM. Compliant with MIPI Alliance Specification for Display Serial Interface	
DSI0_B0_LN0_M	CON1	J16	DSI	AO		
DSI0_C0_LN1_P	CON1	K18	DSI	AO		
DSI0_A1_LN1_M	CON1	J18	DSI	AO		
DSI0_B1_CLK_P	CON1	J17	DSI	AO		
DSI0_C1_CLK_M	CON1	H17	DSI	AO		
DSI0_A2_LN2_P	CON1	J19	DSI	AO		
DSI0_B2_LN2_M	CON1	H19	DSI	AO		
DSI0_C2_LN3_P	CON1	K20	DSI	AO		

DSI0_NC_LN3_M	CON1	J20	DSI	AO		
DSI1_A0_LN0_P	CON1	B26	DSI	AO	MIPI1 Signals for MIPI LCM Compliant with MIPI Alliance Specification for Display Serial Interface	
DSI1_B0_LN0_M	CON1	C26	DSI	AO		
DSI1_C0_LN1_P	CON1	A27	DSI	AO		
DSI1_A1_LN1_M	CON1	B27	DSI	AO		
DSI1_B1_CLK_P	CON1	A25	DSI	AO		
DSI1_C1_CLK_M	CON1	B25	DSI	AO		
DSI1_A2_LN2_P	CON1	B24	DSI	AO		
DSI1_B2_LN2_M	CON1	C24	DSI	AO		
DSI1_C2_LN3_P	CON1	B28	DSI	AO		
DSI1_NC_LN3_M	CON1	C28	DSI	AO		

Table 2.2-3 Display interfaces definition

2.2.4 Camera Interfaces

The SOM supports 6 x 4-lane camera interfaces.

Camera0 Interface						
PIN Name	**Location**	**PIN**	**Voltage**	**Type**	**Description**	**Notes**
CCI_I2C_SDA0	CON1	G28	P3	OD	CCI0 Date signal, already pull up on SOM	
CCI_I2C_SCL0	CON1	G29	P3	OD	CCI0 Clock signal, already pull up on SOM	
CAM_MCLK0	CON1	G12	P3	DO	Camera main clock output	
CSI0_NC_CLK_P	CON1	J11	CSI	AI	MIPI Signals of Camera0 Compliant with MIPI Alliance Standard Specification	
CSI0_A0_CLK_M	CON1	H11	CSI	AI		
CSI0_B0_LN0_P	CON1	J12	CSI	AI		
CSI0_C0_LN0_M	CON1	K12	CSI	AI		
CSI0_A1_LN1_P	CON1	H13	CSI	AI		
CSI0_B1_LN1_M	CON1	J13	CSI	AI		
CSI0_C1_LN2_P	CON1	H15	CSI	AI		
CSI0_A2_LN2_M	CON1	J15	CSI	AI		
CSI0_B2_LN3_P	CON1	J14	CSI	AI		
CSI0_C2_LN3_M	CON1	K14	CSI	AI		
Camera1 Interface						
PIN Name	**Location**	**PIN**	**Voltage**	**Type**	**Description**	**Notes**
CCI_I2C_SDA1	CON1	G30	P3	OD	CCI1 Date signal, already pull up on SOM	
CCI_I2C_SCL1	CON1	G31	P3	OD	CCI1 Clock signal,	

					already pull up on SOM	
CAM_MCLK1	CON1	G14	P3	DO	Camera main clock output	
CSI1_NC_CLK_P	CON1	B17	CSI	AI	MIPI Signals of Camera1 Compliant with MIPI Alliance Standard Specification	
CSI1_A0_CLK_M	CON1	A17	CSI	AI		
CSI1_B0_LN0_P	CON1	C16	CSI	AI		
CSI1_C0_LN0_M	CON1	B16	CSI	AI		
CSI1_A1_LN1_P	CON1	C18	CSI	AI		
CSI1_B1_LN1_M	CON1	B18	CSI	AI		
CSI1_C1_LN2_P	CON1	B15	CSI	AI		
CSI1_A2_LN2_M	CON1	A15	CSI	AI		
CSI1_B2_LN3_P	CON1	C14	CSI	AI		
CSI1_C2_LN3_M	CON1	B14	CSI	AI		

Camera2 Interface

PIN Name	Location	PIN	Voltage	Type	Description	Notes
CCI_I2C_SDA2	CON1	H34	P3	OD	CCI2 Date signal, already pull up on SOM	
CCI_I2C_SCL2	CON1	H35	P3	OD	CCI2 Clock signal, already pull up on SOM	
CAM_MCLK2	CON1	G16	P3	DO	Camera main clock output	
CSI2_NC_CLK_P	CON1	E20	CSI	AI	MIPI Signals of Camera2 Compliant with MIPI Alliance Standard Specification	
CSI2_A0_CLK_M	CON1	F20	CSI	AI		
CSI2_B0_LN0_P	CON1	D19	CSI	AI		
CSI2_C0_LN0_M	CON1	E19	CSI	AI		
CSI2_A1_LN1_P	CON1	E18	CSI	AI		
CSI2_B1_LN1_M	CON1	F18	CSI	AI		
CSI2_C1_LN2_P	CON1	D17	CSI	AI		
CSI2_A2_LN2_M	CON1	E17	CSI	AI		
CSI2_B2_LN3_P	CON1	E16	CSI	AI		
CSI2_C2_LN3_M	CON1	F16	CSI	AI		

Camera3 Interface

CCI_I2C_SDA3	CON1	J35	P3	OD	CCI3 Date signal, already pull up on SOM	
CCI_I2C_SCL3	CON1	H36	P3	OD	CCI3 Clock signal, already pull up on SOM	
CSI3_NC_CLK_P	CON1	C20	CSI	AI	MIPI Signals of Camera3 Compliant with MIPI Alliance Standard Specification	
CSI3_A0_CLK_M	CON1	B20	CSI	AI		
CSI3_B0_LN0_P	CON1	B19	CSI	AI		
CSI3_C0_LN0_M	CON1	A19	CSI	AI		
CSI3_A1_LN1_P	CON1	B23	CSI	AI		

CSI3_B1_LN1_M	CON1	A23	CSI	AI		
CSI3_C1_LN2_P	CON1	C22	CSI	AI		
CSI3_A2_LN2_M	CON1	B22	CSI	AI		
CSI3_B2_LN3_P	CON1	B21	CSI	AI		
CSI3_C2_LN3_M	CON1	A21	CSI	AI		
CAM_MCLK3	CON1	G18	P3	DO	Camera main clock output	
Camera4 Interface						
CSI4_NC_CLK_P	CON1	E24	CSI	AI	MIPI Signals of Camera4 Compliant with MIPI Alliance Standard Specification	
CSI4_A0_CLK_M	CON1	F24	CSI	AI		
CSI4_B0_LN0_P	CON1	D23	CSI	AI		
CSI4_C0_LN0_M	CON1	E23	CSI	AI		
CSI4_A1_LN1_P	CON1	D25	CSI	AI		
CSI4_B1_LN1_M	CON1	E25	CSI	AI		
CSI4_C1_LN2_P	CON1	E22	CSI	AI		
CSI4_A2_LN2_M	CON1	F22	CSI	AI		
CSI4_B2_LN3_P	CON1	D21	CSI	AI		
CSI4_C2_LN3_M	CON1	E21	CSI	AI		
CAM_MCLK4	CON1	G20	P3	DO	Camera main clock output	
Camera5 Interface						
CSI5_NC_CLK_P	CON1	E30	CSI	AI	MIPI Signals of Camera5 Compliant with MIPI Alliance Standard Specification	
CSI5_A0_CLK_M	CON1	F30	CSI	AI		
CSI5_B0_LN0_P	CON1	D27	CSI	AI		
CSI5_C0_LN0_M	CON1	E27	CSI	AI		
CSI5_A1_LN1_P	CON1	D29	CSI	AI		
CSI5_B1_LN1_M	CON1	E29	CSI	AI		
CSI5_C1_LN2_P	CON1	E28	CSI	AI		
CSI5_A2_LN2_M	CON1	F28	CSI	AI		
CSI5_B2_LN3_P	CON1	E26	CSI	AI		
CSI5_C2_LN3_M	CON1	F26	CSI	AI		
CAM_MCLK5	CON1	G24	P3	DO	Camera main clock output	

Table 2.2-4 Camera interface definition

2.2.5 Audio Interface

The SOM provide Soundwire and DMIC interfaces for audio. Soundwire interface is dedicate for external codec IC, which can build system’s audio functions. DMIC interface can be used to directly connect up to 6 PDM MICs.

Audio Interface						
PIN Name	**Location**	**PIN**	**Voltage**	**Type**	**Description**	**Notes**
WCD_SWR_TX_CLK	CON1	K26	P3	DO	Soundwire transmit for WCD	LPI_MI2S0_SCLK
WCD_SWR_TX_DATA0	CON1	K27	P3	DO		LPI_MI2S0_WS
WCD_SWR_TX_DATA1	CON1	K28	P3	DO		LPI_MI2S0_DATA0
WCD_SWR_RX_CLK	CON1	K29	P3	DI	Soundwire receive for WCD	LPI_MI2S0_DATA1
WCD_SWR_RX_DATA0	CON1	K30	P3	DI		LPI_MI2S0_DATA2
WCD_SWR_RX_DATA1	CON1	K31	P3	DI		LPI_MI20_DATA3
WSA_SWR_DATA	CON1	G45	P3	IO	AUDIO PA Soundwire	LPI_MI2S2_WS
WSA_SWR_CLK	CON1	G46	P3	IO		LPI_MI2S2_CLK
DMIC01_CLK	CON1	K43	P3	DO	DMIC I/F	LPI_MI2S1_CLK
DMIC01_DATA	CON1	K44	P3	IO		LPI_MI2S1_WS
DMIC23_CLK	CON1	J43	P3	DO		LPI_MI2S1_DATA0
DMIC23_DATA	CON1	J44	P3	IO		LPI_MI2S1_DATA1
DMIC45_CLK	CON1	J45	P3	DO		LPI_MI2S2_DATA0
DMIC45_DATA	CON1	J46	P3	IO		LPI_M2S2_DATA1
DISPLAY_RESX2/GPIO 136	CON1	K39	P3		I2S1 signals Compliant with Philips I2S Bus Specifications	MI2S0_MCLK
6DOF_L_STROBE/GPIO 138	CON1	D37	P3			MI2S0_SCK
6DOF_R_STROBE/GPIO 139	CON2402	F40	P3			MI2S0_DATA0
GPIO_140	CON2402	D38	P3			MI2S0_DATA1
GPIO_141	CON2402	A10	P3			MI2S0_WS

Table 2.2-5 Audio interface definition

2.2.6 USB & DisplayPort Interface

The SOM support 2 x USB 3.1 GEN2, one can support Type-C with DisplayPort. USB mode and DisplayPort mode can be simultaneously operating at USB 3.1 GEN2 (10 Gbps) and DP 1.4(8.1 Gbps).

PIN Name	Location	PIN	Type	Description	Notes
USB0_SS_RX0_M	CON1	A31	DO	USB 3.0 Signals Compliant with USB 3.1 standard specification	
USB0_SS_RX0_P	CON1	B31	DO		
USB0_SS_RX1_M	CON1	C30	DI		
USB0_SS_RX1_P	CON1	B30	DI		
USB0_SS_TX0_M	CON1	C32	DO		
USB0_SS_TX0_P	CON1	B32	DO		
USB0_SS_TX1_M	CON1	A33	DI		
USB0_SS_TX1_P	CON1	B33	DI		
USB0_HS_DM	CON1	A29	IO	USB 2.0 Signals Compliant with USB 2.0 standard specification	
USB0_HS_DP	CON1	B29	IO		
USB_VBUS	CON1	E47,E48,E49, E50	PO	USB VBUS OTG output	
USB_CC1	CON1	F46	IO	CC pin for Type-C USB connector	
USB_CC2	CON1	E46	IO		
PM855_USB_SBU1	CON1	A43	IO	DP AUX signals	
PM855_USB_SBU2	CON1	A44	IO		
USB1_SS_RX_M	CON1	D33	DI	USB 3.0 Signals Compliant with USB 3.1 standard specification	
USB1_SS_RX_P	CON1	E33	DI		
USB1_SS_TX_M	CON1	E32	DO		
USB1_SS_TX_P	CON1	F32	DO		
USB1_HS_DM	CON1	D31	IO	USB 2.0 Signals Compliant with USB 2.0 standard specification	
USB1_HS_DP	CON1	E31	IO		

Table 2.2-6 USB &DP interface definition

2.2.7 PCIe Interface

The SOM support one Peripheral Component Interconnect Express (PCIe) interfaces, which can be used for general-purpose peripherals.

PIN Name	Location	PIN	Type	Description	Notes
PCIE1_REFCLK_M	CON1	D13	AO	PCIe Signals Compliant with PCI Express Specification Revision 3.0	
PCIE1_REFCLK_P	CON1	E13	AO		
PCIE1_RX0_M	CON1	D11	AI		
PCIE1_RX0_P	CON1	E11	AI		
PCIE1_RX1_M	CON1	E12	AI		

PCIE1_RX1_P	CON1	F12	AI		
PCIE1_TX0_M	CON1	D15	AO		
PCIE1_TX0_P	CON1	E15	AO		
PCIE1_TX1_M	CON1	E14	AO		
PCIE1_TX1_P	CON1	F14	AO		
GPIO_83	CON1	G39	DI	PCIE Clock request	
GPIO_82	CON1	G37	DO	PCIe reset signal	
GPIO_84	CON1	G38	DI	PCIe wake up signal	
PCIE2_REFCLK_M_MDM	CON1	J21	AO	PCIe Signals Compliant with PCI Express Specification Revision 3.0	
PCIE2_REFCLK_P_MDM	CON1	H21	AO		
PCIE2_RX0_M_MDM	CON1	J23	AI		
PCIE2_RX0_P_MDM	CON1	H23	AI		
PCIE2_RX1_M_MDM	CON1	K22	AI		
PCIE2_RX1_P_MDM	CON1	J22	AI		
PCIE2_TX0_M_MDM	CON1	K24	AI		
PCIE2_TX0_P_MDM	CON1	J24	AI		
PCIE2_TX1_M_MDM	CON1	J25	AO		
PCIE2_TX1_P_MDM	CON1	H25	AO		
GPIO_86	CON1	D39	DI	PCIe clock require	
GPIO_85	CON1	F39	DO	PCIe reset signal	

Table 2.2-4 PCIe interface definition

2.2.8 SSC Interface

The SOM has an integrated sensor subsystem called Snapdragon™ sensor core (SSC), which is dedicated to support low-power, always-on use cases.

The sensor subsystem can be left powered on even when the rest of the MSM device is in sleep mode. The SSC has a dedicated 1.5MB L2/TCM cache.

The SSC core has dedicated I/O to communicate with the sensors. The I/O scan support I2C and SPI interfaces.

SSC Interface						
PIN Name	**Location**	**PIN**	**Voltage**	**Type**	**Description**	**Notes**
SNS_I2C0_SDA	CON1	J37	P3	IO	These I2C signals are dedicated to Sensor	GPIO160
SNS_I2C0_SCL	CON1	H37	P3	IO		GPIO161
SNS_I2C4_SDA	CON1	H38	P3	IO	These I2C signals are dedicated to Sensor	GPIO170
SNS_I2C4_SCL	CON1	H39	P3	IO		GPIO171
SPI2_MISO_IMU	CON1	J40	P3	IO	Snapdragon™ Sensor Core SPI signals	GPIO164
SPI2_MOSI_IMU	CON1	J41	P3	IO		GPIO165
SPI2_CLK_IMU	CON1	J38	P3	IO		GPIO166

SPI2_CS_IMU	CON1	J39	P3	IO		GPIO167

Table 3.2-8 SSC interface definition

2.2.9 SDIO Interface

The SOM support dual 4-laneSDIO, SDC2 connect to SD-card.
The SDIO is high-speed signal group. It should protect other sensitive signals/circuits from SD corruption, and protect SD signals from noisy signals (clock, RF and so on).

- The clock can be up to 200 MHz.
- The signals routing should be 50ohm ±10% impedance control.
- CLK to DATA/CMD length matching less than 1mm.
- The spacing to all other signals should 2X line width
- Maximum bus capacitance less than 1.0pF.
- Each trace needs to be next to a ground plane.

SDIO (SDC2) Interface						
PIN Name	**Location**	**PIN**	**Voltage**	**Type**	**Description**	**Notes**
SDC2_CLK_CONN	CON1	B13	P2	DO	SD card signals; SD_UFS_CARD_DET_N need pull up to P3	
SDC2_CMD	CON1	A13	P2	IO		
SDC2_DATA_3	CON1	B11	P2	IO		
SDC2_DATA_2	CON1	A11	P2	IO		
SDC2_DATA_1	CON1	C12	P2	IO		
SDC2_DATA_0	CON1	B12	P2	IO		
SD_UFS_CARD_DET_N	CON1	G43	P3	DI		
SDIO (SDC4) Interface						
PIN Name	**Location**	**PIN**	**Voltage**	**Type**	**Description**	**Notes**
SDC4_DATA0	CON1	A39	P3	IO	SDIO Signals Compliant with SDIO standard specification.	GPIO76
SDC4_DATA1	CON1	A38	P3	IO		GPIO75
SDC4_DATA2	CON1	A4	P3	IO		GPIO74
SDC4_DATA3	CON1	E45	P3	IO		GPIO72
SDC4_CLK	CON1	D44	P3	DO		GPIO73
SDC4_CMD	CON1	E44	P3	IO		GPIO71

Table 2.2-8 SDIO interface definition

2.2.10 QUP Interface

These GPIOs are available as Qualcomm universal peripheral (QUP) interface ports that can be configured for UART, SPI, I2C or I3C operation.

I2C is a two-wire bus that can be routed to multiple devices; each line of each bus need to supplement by a 2.2kΩ pull-up resistor

QUP Interface

PIN Name	Location	PIN	Voltage	Type	Description	Notes
GPIO0	CON1	K32	P3	IO	QUP19 can be configured to GPIO or UART or SPI or I2C	
GPIO1	CON1	E39	P3	IO		
GPIO2	CON1	F38	P3	IO		
GPIO3	CON1	E38	P3	IO		
GPIO4	CON1	H33	P3	IO	QUP1 can be configured to GPIO or UART or SPI or I2C	
GPIO5	CON1	H31	P3	IO		
GPIO6	CON1	H30	P3	IO		
GPIO7	CON1	H32	P3	IO		
GPIO12	CON1	B9	P3	IO	QUP5 can be configured to GPIO or SPI or I2C	
GPIO13	CON1	B10	P3	IO		
GPIO14	CON1	J27	P3	IO		
GPIO15	CON1	J28	P3	IO		
GPIO24	CON1	G32	P3	IO	QUP8 can be configured to GPIO or UART or I3C or SPI or I2C	
GPIO25	CON1	J36	P3	IO		
GPIO26	CON1	K36	P3	IO		
SDM_FAST_BOOT_0	CON1	B47	P3	IO		GPIO27
GPIO28	CON1	H29	P3	IO	QUP0 can be configured to GPIO or UART or I3C or SPI or I2C	
GPIO29	CON1	H28	P3	IO		
GPIO30	CON1	H27	P3	IO		
GPIO31	CON1	H26	P3	IO		
TS_I2C_SDA	CON1	E42	P3	IO	QUP13 can be configured to GPIO or SPI or I2C	GPIO36
TS_I2C_SCL	CON1	D41	P3	IO		GPIO37
TS_RESET_N	CON1	D42	P3	IO		GPIO38
TS_INT_N	CON1	D40	P3	IO		GPIO39
FP_SPI_MISO	CON1	C37	P3	IO	QUP14 can be configured to GPIO or UART or I3C or SPI or I2C	GPIO40
FP_SPI_MOSI	CON1	B37	P3	IO		GPIO41
FP_SPI_CLK	CON1	B36	P3	IO		GPIO42
FP_SPI_CS	CON1	C36	P3	IO		GPIO43
APPS_I2C_SDA	CON1	F44	P3	IO	QUP15 can be configured to GPIO or SPI or I2C	GPIO44
APPS_I2C_SCL	CON1	E43	P3	IO		GPIO45
MIPI_ERR_FG	CON1	E41	P3	IO		GPIO46
SDM_FAST_BOOT_1	CON1	E40	P3	IO		GPIO47
GPIO52	CON1	G36	P3	IO	QUP17 can be	

GPIO53	CON1	F37	P3	IO	configured to GPIO or SPI or I2C	
GPIO54	CON1	C42	P3	IO		
GPIO55	CON1	F36	P3	IO		
GPIO56	CON1	G35	P3	IO	QUP18 can be configured to GPIO or SPI or I2C	
GPIO57	CON1	F34	P3	IO		
GPIO58	CON1	G34	P3	IO		
GPIO59	CON1	G33	P3	IO		
GPIO8	CON1	A46	P3	IO	QUP4 can be configured to GPIO or I2C	
GPIO9	CON1	D35	P3	IO		
RGB_1V2_EN	CON1	K40	P3	IO	QUP2 can be configured to GPIO or I2C	GPIO 115
GPIO 116	CON1	K41	P3	IO		GPIO 116
GPIO125	CON1	A9	P3	IO	QUP9 can be configured to GPIO or I2C	
6DOF_ULPM	CON1	B45	P3	IO		GPIO 126
WSA2_EN	CON1	B41	P3	IO	QUP10 can be configured to GPIO or I2C	GPIO 129
6DOF_L_RST	CON1	B44	P3	IO		GPIO 130

Table 3.2-5 QUP interface definition

2.2.11 Power on Interface

Dedicated PMIC circuits continuously monitor events that might trigger a power-on sequence. If an event occurs, these circuits power on the IC, determine the device's available power sources, enable the correct source. It is longer than 1s with pressing power-on key, for power on event. And it is suggested for 3s powering on system. Power on/off key signal can be connected to ground through CON1.A45; the other power on method is: when using CBL_PWR_N pin connect to ground, insert battery or power supply， SOM will power on automatically.

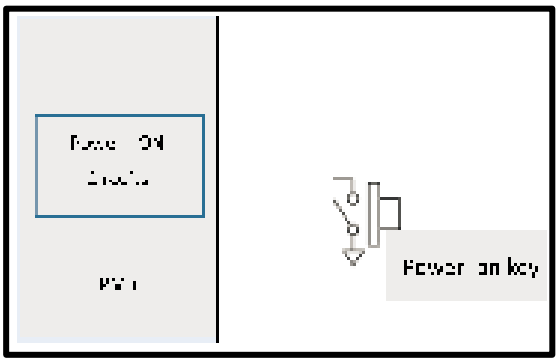

Figure 3.2-1 Power on signal

Power on Interface						
PIN Name	**Location**	**PIN**	**Voltage**	**Type**	**Description**	**Notes**

CBL_PWR_N	CON1	A45	pulled up internally through a 200K resistor to 1.8V	DI	Signal use for auto power on when you plug in a battery, active low, internal pull up	

Table 3.2-11 Power on interface definition

2.2.12 Reset Interface

Extended press of volume key will initiate a shutdown or reset (software selectable)

- Stage 1 reset – software-configurable bark

PMIC generates interrupt, giving the MSM device the opportunity to fix the problem or gracefully reset the system. Example events that can cause a bark: Over temperature indicates system is getting too hot. PMIC watchdog indicates that it has not kicked.

- Stage 2 –software-configurable bite

If reset is ignored, PMIC will force a reset event (selectable by software).

- Stage 3 –hardware mandatory bite

The user can generate a mandatory reset by a long press of PM_RESIN_N, or PHONE_ON_N, or PM_RESIN_N + PHONE_ON_N in combination.

The standalone or combination of reset triggers can also be selected as SBL by directly writing to the appropriate registers

Reset Pin						
PIN Name	**Location**	**PIN**	**Voltage**	**Type**	**Description**	**Notes**
PM_RESIN_N	CON1	A42	pulled up internally to 1.8V	DI	Volume down/Reset key signal, Low active	

Table 3.2-12 Reset interface definition

2.2.13 Keys Interface

This is interface dedicate for key.

KEYs PINs						
PIN Name	**Location**	**PIN**	**Voltage**	**Type**	**Description**	**Notes**
PHONE_ON_N	CON1	A40	P3	DI	Power on key signal, Low active	
PM_RESIN_N	CON1	A42	P3	DI	Volume down/Reset key	

					signal, Low active	
VOL_UP_N	CON1	A41	P3	DI	Volume up key signal, Low active	

Table 3.2-6 Keys interface definition

2.2.14 Sensor Interrupt Interface

All these interfaces dedicate to below sensors.

Sensor Interrupt PINs						
PIN Name	**Location**	**PIN**	**Voltage**	**Type**	**Description**	**Notes**
SEN1_ACCL_INT1	CON1	J33	P3	DI	Accelerometer sensor interrupt	
SEN1_GYRO_INT2	CON1	J32	P3	DI	Gyroscope sensor interrupt	
ALPS_INT_N	CON1	J29	P3	DI	Proximity sensor interrupt	

Table 3.2-7 Sensor interrupt definition

2.2.15 Debug UART Interface

This is interface dedicate for debug.

Debug UART PINs						
PIN Name	**Location**	**PIN**	**Voltage**	**Type**	**Description**	**Notes**
SDM_DEBUG_UART_TX	CON1	B46	P3	DI	QUP12 UART signals, can use for debug	
SDM_DEBUG_UART_RX	CON1	C45	P3	DO		

Table 3.2-8 Debug UART interface definition

2.2.16 Battery Interface

This is dedicate for battery interface, major for monitoring battery status, inserting and voltage detect.

Battery PINs						
PIN Name	**Location**	**PIN**	**Voltage**	**Type**	**Description**	**Notes**
VBATT_CONN_VSENSE_P	CON1	H47	VBATT	AI	Battery voltage sense positive input signal	
VBATT_CONN_VSENSE_M	CON1	G47	VBATT	AI	Battery voltage sense negative input signal	
BATT_THERM	CON1	K46	0~1.875V	AI	Battery temperature sense input signal	

BATT_ID	CON1	K45	0~1.875V	AI	Battery ID sense input signal	

Table 3.2-9 Battery interface definition

2.2.17 ADCs Interface

The ADC input signal use as analog multiplexer function.

ADCs PINs						
PIN Name	**Location**	**PIN**	**Voltage**	**Type**	**Description**	**Notes**
PM_GPIO5	CON1	A6	0~1.875V	LV	ADC input, can be configured as 1.8V	PM8150L_GPIO5
GPIO_6_PWM	CON1	K38	0~1.875V	LV	ADC input, can be configured as 1.8V	PM8150L_GPIO6
PM_GPIO7	CON1	A7	0~5V	MV	ADC input, can be configured as 1.8V or 5V	PM8150L_GPIO7
PM_GPIO10	CON1	A8	0~5V	MV	ADC input, can be configured as 1.8V or 5V	PM8150L_GPIO10

Table 3.2-1710 MPPs interface definition

2.2.18 PWMs and LED Current Driver Interface

The SOM support dual PWM output and dual LED Current Driver, all PWM output by Light Pulse Generators.

LED Current Driver PINs can be used for different events, they are separate controller. Independently programmable duty cycle and period via LPGs (6-or 9-bit resolution) for digital dimming.

PWMs PINs						
PIN Name	**Location**	**PIN**	**Voltage**	**Type**	**Description**	**Notes**
GPIO_6_PWM	CON1	K38	0~1.875V	LV	Can be configured as GPIO and PWM(max 19.2MHz)	PM8150L_GPIO6
PM_GPIO10	CON1	A8	0~5V	MV		PM8150L_GPIO10
LED Driver PINs						
PIN Name	**Location**	**PIN**	**Voltage**	**Type**	**Description**	**Notes**
R_LED	CON1	H46		AO	Custom indicator light, connect to positive port	LPG_OUT_1
B_LED	CON1	H44		AO	Custom indicator light, connect to positive port	LPG_OUT_3
G_LED	CON1	H45		AO	Custom indicator light,	LPG_OUT_2

					connect to positive port	

Table 3.2-11 PWMs and LED Current Driver interface definition

2.2.19 Antenna Interface

The SOM provides the fully-integrated WLAN and Bluetooth function.
The WLAN and Bluetooth share the antenna port with 50ohm impedance.

- WLAN supports 2 × 2 multiple input, multiple output (MIMO) with two spatial streams IEEE802.11 a/b/g/n/ac/ax WLAN standards.
- Supports Bluetooth 5.1 + HS enabling seamless integration of WLAN/Bluetooth and low energy technology.

Antenna interface						
Name	**Location**	**PIN**	**Voltage**	**Type**	**Description**	**Notes**
Antenna 1	J1501			IO	Antenna 1 supports WIFI 2.4G/5G &BT	Chain0
Antenna 2	J5907			IO	Antenna 2 supports WIFI 2.4G/5G	Chain1

Table 3.2-12 Antenna interface definition

3 Connector PIN Summary

3.1 CON1 BTB Connector

Pin#	Function	Function description
A1	GND	GND
A2	RF_CH0_CON	WiFi 2.4/5G RF out, Chain0
A3	GND	GND
A4	GPIO_74	GPIO 74
A5	GND	GND
A6	PM_GPIO5	PM8150L GPIO 5
A7	PM_GPIO7	PM8150L GPIO 7
A8	PM_GPIO10	PM8150L GPIO 10
A9	GPIO_125	GPIO 125
A10	GPIO_141	GPIO 141
A11	SDC2_DATA_2	Secure digital controller 2 data bit 2
A12	GND	GND
A13	SDC2_CMD	Secure digital controller 2 command
A14	GND	GND
A15	CSI1_A2_LN2_M	MIPI CSI 1 (DPHY), differential lane 2 – minus
A16	GND	GND
A17	CSI1_A0_CLK_M	MIPI CSI 1 (DPHY), differential clock – minus
A18	GND	GND
A19	CSI3_C0_LN0_M	MIPI CSI 3 (DPHY), differential lane 0 – minus
A20	GND	GND
A21	CSI3_C2_LN3_M	MIPI CSI 3 (DPHY), differential lane 3 – minus
A22	GND	GND
A23	CSI3_B1_LN1_M	MIPI CSI 3 (DPHY), differential lane 1 – minus
A24	GND	GND
A25	DSI1_B1_CLK_P	MIPI DSI 1 (DPHY), differential clock – plus
A26	GND	GND
A27	DSI1_C0_LN1_P	MIPI DSI 1 (DPHY), differential lane 1 – plus
A28	GND	GND
A29	USB0_HS_DM	USB high-speed 0 data – minus
A30	GND	GND
A31	USB0_SS_RX0_M	USB super-speed 0 receive 0 – minus
A32	GND	GND
A33	USB0_SS_TX1_M	USB super-speed 0 transmit 1 – minus
A34	GND	GND
A35	PMK8002_RF_CLK1	RF clock 1 for PMK8002
A36	GND	GND

A37	PMK8002_RF_CLK2	RF clock 2 for PMK8002
A38	DISP0_RESET_N	LCM reset
A39	SDM_FAST_BOOT_2	Boot configuration 2
A40	DEBUG_PMIC_PKD_N	Power key
A41	DEBUG_KEY_VOL_UP_N	Volume up key
A42	DEBUG_KEY_VOL_DOWN_N	Volume down key
A43	PM855_USB_SBU1	SBU1 of Type C
A44	PM855_USB_SBU2	SBU2 of Type C
A45	CBL_PWR_N	CBL_PWR
A46	GPIO_8_C	GPIO 8
A47	VDISP_P_OUT	LCM Backlight Positive
A48	VDISP_M_OUT	LCM Backlight Minus
A49	VREG_L11C_3P3	VREG_L11C_3P3
A50	VREG_L9C_2P96	VREG_L9C_2P96
B1	GPIO_168	GPIO 168
B2	GND	GND
B3	GND	GND
B4	VREG_L5C_1P8	VREG_L5C_1P8
B5	VREG_L5C_1P8	VREG_L5C_1P8
B6	GPIO_135	GPIO 135
B7	GPIO_162	GPIO 162
B8	GPIO_163	GPIO 163
B9	GPIO_12	GPIO 12
B10	GPIO_13	GPIO 13
B11	SDC2_DATA_3	Secure digital controller 2 data bit 3
B12	SDC2_DATA_0	Secure digital controller 2 data bit 0
B13	SDC2_CLK_CONN	Secure digital controller 2 clock
B14	CSI1_C2_LN3_M	MIPI CSI 1 (DPHY), differential lane 3 – minus
B15	CSI1_C1_LN2_P	MIPI CSI 1 (DPHY), differential lane 2 – plus
B16	CSI1_C0_LN0_M	MIPI CSI 1 (DPHY), differential lane 0 – minus
B17	CSI1_NC_CLK_P	MIPI CSI 1 (DPHY), differential clock – plus
B18	CSI1_B1_LN1_M	MIPI CSI 1 (DPHY), differential lane 1 – minus
B19	CSI3_B0_LN0_P	MIPI CSI 3 (DPHY), differential lane 0 – plus
B20	CSI3_A0_CLK_M	MIPI CSI 3 (DPHY), differential clock – minus
B21	CSI3_B2_LN3_P	MIPI CSI 3 (DPHY), differential lane 3 – plus
B22	CSI3_A2_LN2_M	MIPI CSI 3 (DPHY), differential lane 2 – minus
B23	CSI3_A1_LN1_P	MIPI CSI 3 (DPHY), differential lane 1 – plus
B24	DSI1_A2_LN2_P	MIPI DSI 1 (DPHY), differential lane 2 – plus
B25	DSI1_C1_CLK_M	MIPI DSI 1 (DPHY), differential clock – minus
B26	DSI1_A0_LN0_P	MIPI DSI 1 (DPHY), differential lane 0 – plus
B27	DSI1_A1_LN1_M	MIPI DSI 1 (DPHY), differential lane 1 – minus
B28	DSI1_C2_LN3_P	MIPI DSI 1 (DPHY), differential lane 3 – plus
B29	USB0_HS_DP	USB high-speed 0 data – plus

B30	USB0_SS_RX1_P	USB super-speed 0 receive 1 – plus
B31	USB0_SS_RX0_P	USB super-speed 0 receive 0 – plus
B32	USB0_SS_TX0_P	USB super-speed 0 transmit 0 – plus
B33	USB0_SS_TX1_P	USB super-speed 0 transmit 1 – plus
B34	DP_AUX_P	AUX P for DP
B35	PMK8002_PMIC_CLK	clock for PMK8002
B36	FP_SPI_CLK	SPI clock
B37	FP_SPI_MOSI	SPI MOSI
B38	MDM_SKIN_THERM	Thermal sensor for RF
B39	GPIO_9_P	GPIO 9
B40	WSA1_EN	Audio PA sound wire enable 1
B41	WSA2_EN	Audio PA sound wire enable 2
B42	VREG_L8C_1P8	VREG_L8C_1P8
B43	VREG_IO_1P8	VREG_IO_1P8
B44	6DOF_L_RST	GPIO 130
B45	6DOF_ULPM	GPIO 126
B46	SDM_DEBUG_UART_TX	Uart TX for system debug
B47	SDM_FAST_BOOT_0	Boot configuration 0
B48	GND	GND
B49	GND	GND
B50	GND	GND
C1	GND	GND
C2	RF_CLK1	RF CLOCK
C3	GND	GND
C4	NC	NC
C5	PM8250_GPIO3	PM8250 GPIO 3
C6	NC	NC
C7	PM8150L_AMUX1	Analog Multiplexer input
C8	NC	NC
C9	PM8150B_AMUX1	Analog Multiplexer input
C10	NC	NC
C11	GND	GND
C12	SDC2_DATA_1	Secure digital controller 2 data bit 1
C13	GND	GND
C14	CSI1_B2_LN3_P	MIPI CSI 1 (DPHY), differential lane 3 – plus
C15	GND	GND
C16	CSI1_B0_LN0_P	MIPI CSI 1 (DPHY), differential lane 0 – plus
C17	GND	GND
C18	CSI1_A1_LN1_P	MIPI CSI 1 (DPHY), differential lane 1 – plus
C19	GND	GND
C20	CSI3_NC_CLK_P	MIPI CSI 3 (DPHY), differential clock – plus
C21	GND	GND
C22	CSI3_C1_LN2_P	MIPI CSI 3 (DPHY), differential lane 2 – plus

C23	GND	GND
C24	DSI1_B2_LN2_M	MIPI DSI 1 (DPHY), differential lane 2 – minus
C25	GND	GND
C26	DSI1_B0_LN0_M	MIPI DSI 1 (DPHY), differential lane 0 – minus
C27	GND	GND
C28	DSI1_NC_LN3_M	MIPI DSI 1 (DPHY), differential lane 3 – minus
C29	GND	GND
C30	USB0_SS_RX1_M	USB super-speed 0 receive 1 – minus
C31	GND	GND
C32	USB0_SS_TX0_M	USB super-speed 0 transmit 0 – minus
C33	GND	GND
C34	DP_AUX_N	AUX N for DP
C35	GND	GND
C36	FP_SPI_CS	SPI selection
C37	FP_SPI_MISO	SPI MISO
C38	FSA_INT_N	GPIO 63
C39	GPIO_10_P	GPIO 10
C40	GPIO_88	GPIO 88
C41	GPIO_89	GPIO 89
C42	GPIO_54	GPIO 54
C43	SDM_FORCE_USB_BOOT	Force boot configuration
C44	6DOF_R_RS	GPIO
C45	SDM_DEBUG_UART_RX	Uart RX for system debug
C46	WCD_RESET_N	SoundWire reset
C47	GND	GND
C48	GND	GND
C49	GND	GND
C50	GND	GND
D1	NC	NC
D2	GND	GND
D3	RF_CH1_CON	WiFi 2.4/5G RF out, Chain1
D4	GND	GND
D5	SDM_WDOG_DISABLE	GPIO 128
D6	NC	NC
D7	GPIO_137	GPIO 137
D8	NC	NC
D9	NC	NC
D10	NC	NC
D11	PCIE1_RX0_M	PCIe 1 Gen 3 receive 0 – minus
D12	GND	GND
D13	PCIE1_REFCLK_M	PCIe 1 Gen 3 reference clock – minus
D14	GND	GND
D15	PCIE1_TX0_M	PCIe 1 Gen 3 transmit 0 – minus

D16	GND	GND
D17	CSI2_C1_LN2_P	MIPI CSI 2 (DPHY), differential lane 2 – plus
D18	GND	GND
D19	CSI2_B0_LN0_P	MIPI CSI 2 (DPHY), differential lane 0 – plus
D20	GND	GND
D21	CSI4_B2_LN3_P	MIPI CSI 4 (DPHY), differential lane 3 – plus
D22	GND	GND
D23	CSI4_B0_LN0_P	MIPI CSI 4 (DPHY), differential lane 0 – plus
D24	GND	GND
D25	CSI4_A1_LN1_P	MIPI CSI 4 (DPHY), differential lane 1 – plus
D26	GND	GND
D27	CSI5_B0_LN0_P	MIPI CSI 5 (DPHY), differential lane 0 – plus
D28	GND	GND
D29	CSI5_A1_LN1_P	MIPI CSI 5 (DPHY), differential lane 1 – plus
D30	GND	GND
D31	USB1_HS_DM	USB high-speed 1 data – minus
D32	GND	GND
D33	USB1_SS_RX_M	USB super-speed 1 receive – minus
D34	GND	GND
D35	GPIO_9_C	GPIO 9
D36	GPIO_64	GPIO 64
D37	6DOF_L_STROBE	GPIO 138
D38[note1]	GPIO_140_CON	See below table
D39	GPIO_86	GPIO 86
D40	TS_INT_N	GPIO 39
D41	TS_I2C_SCL	Clock of I2C
D42	TS_RESET_N	GPIO 38
D43	VREG_L2A_3P1	VREG_L2A_3P1
D44	GPIO_73_C	GPIO 73
D45	VREG_S4A_1P8	VREG_S4A_1P8
D46	VREG_S4A_1P8	VREG_S4A_1P8
D47	VREG_BOB	VREG_BOB
D48	VREG_BOB	VREG_BOB
D49	VPH_PWR	Vsystem. Power supply for function module.
D50	VPH_PWR	Vsystem. Power supply for function module.
E1	NC	NC
E2	NC	NC
E3	GND	GND
E4	NC	NC
E5	NC	NC
E6	NC	NC
E7	NC	NC
E8	NC	NC

E9	NC	NC
E10	NC	NC
E11	PCIE1_RX0_P	PCIe 1 Gen 3 receive 0 – plus
E12	PCIE1_RX1_M	PCIe 1 Gen 3 receive 1 – minus
E13	PCIE1_REFCLK_P	PCIe 1 Gen 3 reference clock – plus
E14	PCIE1_TX1_M	PCIe 1 Gen 3 transmit 1 – minus
E15	PCIE1_TX0_P	PCIe 1 Gen 3 transmit 0 – plus
E16	CSI2_B2_LN3_P	MIPI CSI 2 (DPHY), differential lane 3 – plus
E17	CSI2_A2_LN2_M	MIPI CSI 2 (DPHY), differential lane 2 – minus
E18	CSI2_A1_LN1_P	MIPI CSI 2 (DPHY), differential lane 1 – plus
E19	CSI2_C0_LN0_M	MIPI CSI 2 (DPHY), differential lane 0 – minus
E20	CSI2_NC_CLK_P	MIPI CSI 2 (DPHY), differential clock – plus
E21	CSI4_C2_LN3_M	MIPI CSI 4 (DPHY), differential lane 3 – minus
E22	CSI4_C1_LN2_P	MIPI CSI 4 (DPHY), differential lane 2 – plus
E23	CSI4_C0_LN0_M	MIPI CSI 4 (DPHY), differential lane 0 – minus
E24	CSI4_NC_CLK_P	MIPI CSI 4 (DPHY), differential clock – plus
E25	CSI4_B1_LN1_M	MIPI CSI 4 (DPHY), differential lane 1 – minus
E26	CSI5_B2_LN3_P	MIPI CSI 5 (DPHY), differential lane 3 – plus
E27	CSI5_C0_LN0_M	MIPI CSI 5 (DPHY), differential lane 0 – minus
E28	CSI5_C1_LN2_P	MIPI CSI 5 (DPHY), differential lane 2 – plus
E29	CSI5_B1_LN1_M	MIPI CSI 5 (DPHY), differential lane 1 – minus
E30	CSI5_NC_CLK_P	MIPI CSI 5 (DPHY), differential clock – plus
E31	USB1_HS_DP	USB high-speed 1 data – plus
E32	USB1_SS_TX_M	USB super-speed 1 receive – plus
E33	USB1_SS_RX_P	USB super-speed 1 receive – plus
E34	PMIC_SPMI_CLK	SPMI clock
E35	PMIC_SPMI_DATA	SPMI data
E36	GPIO_10_C	GPIO 10
E37[note1]	GPIO 145	See below table
E38	GPIO_3	GPIO 3
E39	GPIO_1	GPIO 1
E40	SDM_FAST_BOOT_1	Boot configuration 1
E41	MIPI_ERR_FG	GPIO 46
E42	TS_I2C_SDA	Data of I2C
E43	APPS_I2C_SCL	I2C SCL for sensor
E44	GPIO_71_C	GPIO 71
E45	GPIO_72_C	GPIO 72
E46	USB_CC2	CC2 of Type C
E47	USB_VBUS	VBUS of Type C
E48	USB_VBUS	VBUS of Type C
E49	USB_VBUS	VBUS of Type C
E50	USB_VBUS	VBUS of Type C
F1	NC	NC

F2	NC	NC
F3	NC	NC
F4	NC	NC
F5	NC	NC
F6	NC	NC
F7	NC	NC
F8	NC	NC
F9	NC	NC
F10	NC	NC
F11	GND	GND
F12	PCIE1_RX1_P	PCIe 1 Gen 3 receive 1 – plus
F13	GND	GND
F14	PCIE1_TX1_P	PCIe 1 Gen 3 transmit 1 – plus
F15	GND	GND
F16	CSI2_C2_LN3_M	MIPI CSI 2 (DPHY), differential lane 3 – minus
F17	GND	GND
F18	CSI2_B1_LN1_M	MIPI CSI 2 (DPHY), differential lane 1 – minus
F19	GND	GND
F20	CSI2_A0_CLK_M	MIPI CSI 2 (DPHY), differential clock – minus
F21	GND	GND
F22	CSI4_A2_LN2_M	MIPI CSI 4 (DPHY), differential lane 2 – minus
F23	GND	GND
F24	CSI4_A0_CLK_M	MIPI CSI 4 (DPHY), differential clock – minus
F25	GND	GND
F26	CSI5_C2_LN3_M	MIPI CSI 5 (DPHY), differential lane 3 – minus
F27	GND	GND
F28	CSI5_A2_LN2_M	MIPI CSI 5 (DPHY), differential lane 2 – minus
F29	GND	GND
F30	CSI5_A0_CLK_M	MIPI CSI 5 (DPHY), differential clock – minus
F31	GND	GND
F32	USB1_SS_TX_P	USB super-speed 1 transmit – plus
F33	GND	GND
F34	GPIO_57	GPIO 57
F35	GND	GND
F36	GPIO_55	GPIO 55
F37	GPIO_53	GPIO 53
F38	GPIO_2	GPIO 2
F39	GPIO_85	GPIO 85
F40	6DOF_R_STROBE	GPIO 139
F41	SLEEP_CLK	Sleep clock
F42	CONFIRM	PM8250 GPIO 7
F43	MDP_VSYNC_P	GPIO 66
F44	APPS_I2C_SDA	I2C SDA for sensor

F45	PM_FAULT_N	FAULT_N for PMIC
F46	USB_CC1	CC1 of Type C
F47	GND	GND
F48	GND	GND
F49	GND	GND
F50	GND	GND
G1	NC	NC
G2	NC	NC
G3	NC	NC
G4	NC	NC
G5	NC	NC
G6	NC	NC
G7	NC	NC
G8	NC	NC
G9	NC	NC
G10	NC	NC
G11	GND	GND
G12	CAM_MCLK0	Camera master clock 0
G13	GND	GND
G14	CAM_MCLK1	Camera master clock 1
G15	GND	GND
G16	CAM_MCLK2	Camera master clock 2
G17	GND	GND
G18	CAM_MCLK3	Camera master clock 3
G19	GND	GND
G20	CAM_MCLK4	Camera master clock 4
G21	GND	GND
G22	CAM_MCLK6	Camera master clock 6
G23	GND	GND
G24	CAM_MCLK5	Camera master clock 5
G25	GND	GND
G26	CAM2_RST_N	Camera 2 reset
G27	GND	GND
G28	CCI_I2C_SDA0	Dedicated camera control interface I2C 0 serial data
G29	CCI_I2C_SCL0	Dedicated camera control interface I2C 0 clock
G30	CCI_I2C_SDA1	Dedicated camera control interface I2C 1 serial data
G31	CCI_I2C_SCL1	Dedicated camera control interface I2C 1 clock
G32	GPIO_24	GPIO 24
G33	GPIO_59	GPIO 59
G34	GPIO_58	GPIO 58
G35	GPIO_56	GPIO 56
G36	GPIO_52	GPIO 52
G37	6DOF_1V2_EN	GPIO 82

G38	6DOF_2V8_EN	GPIO 84
G39	6DOF_1V8_EN	GPIO 83
G40	GPIO_22_C	GPIO 22
G41	GPIO_23	GPIO 23
G42	CAM1_RST_N	Camera 1 reset, GPIO 92
G43	SD_UFS_CARD_DET_N	SD CARD detection, GPIO 77
G44	GPIO_144_C	GPIO 144
G45	WSA_SWR_DATA	Audio PA sound wire data
G46	WSA_SWR_CLK	Audio PA sound wire clock
G47	VBATT_CONN_VSENSE_M	Battery current sense minus
G48	GND	GND
G49	GND	GND
G50	GND	GND
H1	NC	NC
H2	NC	NC
H3	NC	NC
H4	NC	NC
H5	NC	NC
H6	NC	NC
H7	NC	NC
H8	NC	NC
H9	NC	NC
H10	NC	NC
H11	CSI0_A0_CLK_M	MIPI CSI 0 (DPHY), differential clock – minus
H12	GND	GND
H13	CSI0_A1_LN1_P	MIPI CSI 0 (DPHY), differential lane 1 – plus
H14	GND	GND
H15	CSI0_C1_LN2_P	MIPI CSI 0 (DPHY), differential lane 2 – plus
H16	GND	GND
H17	DSI0_C1_CLK_M	MIPI DSI 0 (DPHY), differential clock – minus
H18	GND	GND
H19	DSI0_B2_LN2_M	MIPI DSI 0 (DPHY), differential lane 2 – minus
H20	GND	GND
H21	PCIE2_REFCLK_P_MDM	PCIe 2 Gen3 reference clock - plus
H22	GND	GND
H23	PCIE2_RX0_P_MDM	PCIe 2 Gen 3 receive 0 - plus
H24	GND	GND
H25	PCIE2_TX1_P_MDM	PCIe 2 Gen 3 transmit 1 - plus
H26	GPIO_31	GPIO 31
H27	GPIO_30	GPIO 30
H28	GPIO_29	GPIO 29
H29	GPIO_28	GPIO 28
H30	GPIO_6	GPIO 6

H31	GPIO_5	GPIO 5
H32	GPIO_7	GPIO 7
H33	GPIO_4	GPIO 4
H34	CCI_I2C_SDA2	Dedicated camera control interface I2C 2 serial data
H35	CCI_I2C_SCL2	Dedicated camera control interface I2C 2 clock
H36	CCI_I2C_SCL3	Dedicated camera control interface I2C 3 clock
H37	SNS_I2C0_SCL	Clock of I2C0, for sensor
H38	SNS_I2C4_SDA	Data of I2C4, for sensor
H39	SNS_I2C4_SCL	Clock of I2C4, for sensor
H40	GPIO_173	GPIO 173
H41	GPIO_174	GPIO 174
H42	GPIO_175	GPIO 175
H43	GPIO_172	GPIO 172
H44	B_LED	LED positive
H45	G_LED	LED positive
H46	R_LED	LED positive
H47	VBATT_CONN_VSENSE_P	Battery current sense positive
H48	GND	GND
H49	GND	GND
H50	GND	GND
J1	NC	NC
J2	NC	NC
J3	NC	NC
J4	NC	NC
J5	NC	NC
J6	NC	NC
J7	NC	NC
J8	NC	NC
J9	NC	NC
J10	NC	NC
J11	CSI0_NC_CLK_P	MIPI CSI 0 (DPHY), differential clock – plus
J12	CSI0_B0_LN0_P	MIPI CSI 0 (DPHY), differential lane 0 – plus
J13	CSI0_B1_LN1_M	MIPI CSI 0 (DPHY), differential lane 1 – minus
J14	CSI0_B2_LN3_P	MIPI CSI 0 (DPHY), differential lane 3 – plus
J15	CSI0_A2_LN2_M	MIPI CSI 0 (DPHY), differential lane 2 – minus
J16	DSI0_B0_LN0_M	MIPI DSI 0 (DPHY), differential lane 0 – minus
J17	DSI0_B1_CLK_P	MIPI DSI 0 (DPHY), differential clock – plus
J18	DSI0_A1_LN1_M	MIPI DSI 0 (DPHY), differential lane 1 – minus
J19	DSI0_A2_LN2_P	MIPI DSI 0 (DPHY), differential lane 2 – plus
J20	DSI0_NC_LN3_M	MIPI DSI 0 (DPHY), differential lane 3 – minus
J21	PCIE2_REFCLK_M_MDM	PCIe 2 Gen3 reference clock - minus
J22	PCIE2_RX1_P_MDM	PCIe 2 Gen 3 receive 1 - plus
J23	PCIE2_RX0_M_MDM	PCIe 2 Gen 3 receive 0 - minus

J24	PCIE2_TX0_P_MDM	PCIe 2 Gen 3 transmit 0 - plus
J25	PCIE2_TX1_M_MDM	PCIe 2 Gen 3 transmit 1 - minus
J26	CABC	CABC
J27	GPIO_14	GPIO 14
J28	GPIO_15	GPIO 15
J29	ALPS_INT_N	interrupter
J30	EYETCK_2V8_EN	GPIO 114
J31	CAM3_RST_N	Camera 3 reset, GPIO109
J32	SEN1_GYRO_INT2	Sensor Interrupt, GPIO 113
J33	SEN1_ACCL_INT1	Sensor Interrupt, GPIO 112
J34	TE	TE for LCM, GPIO 67
J35	CCI_I2C_SDA3	Dedicated camera control interface I2C 3 serial data
J36	GPIO_25	GPIO 25
J37	SNS_I2C0_SDA	Data of I2C0, for sensor
J38	SPI2_CLK_IMU	SPI clock, for sensor
J39	SPI2_CS_IMU	SPI selection, for sensor
J40	SPI2_MISO_IMU	SPI MISO, for sensor
J41	SPI2_MOSI_IMU	SPI MOSI, for sensor
J42	GPIO_87	GPIO 87
J43	DMIC23_CLK	DMIC2/3 clock
J44	DMIC23_DATA	DMIC2/3 data
J45	DMIC45_CLK	DMIC4/5 clock
J46	DMIC45_DATA	DMIC4/5 data
J47	VBAT_CON	VBAT
J48	VBAT_CON	VBAT
J49	VBAT_CON	VBAT
J50	VBAT_CON	VBAT
K1	NC	NC
K2	NC	NC
K3	NC	NC
K4	NC	NC
K5	NC	NC
K6	NC	NC
K7	NC	NC
K8	NC	NC
K9	NC	NC
K10	NC	NC
K11	GND	GND
K12	CSI0_C0_LN0_M	MIPI CSI 0 (DPHY), differential lane 0 – minus
K13	GND	GND
K14	CSI0_C2_LN3_M	MIPI CSI 0 (DPHY), differential lane 3 – minus
K15	GND	GND
K16	DSI0_A0_LN0_P	MIPI DSI 0 (DPHY), differential lane 0 – plus

K17	GND	GND
K18	DSI0_C0_LN1_P	MIPI DSI 0 (DPHY), differential lane 1 – plus
K19	GND	GND
K20	DSI0_C2_LN3_P	MIPI DSI 0 (DPHY), differential lane 3 – plus
K21	GND	GND
K22	PCIE2_RX1_M_MDM	PCIe 2 Gen 3 receive 1 - minus
K23	GND	GND
K24	PCIE2_TX0_M_MDM	PCIe 2 Gen 3 transmit 0 - minu
K25	GND	GND
K26	WCD_SWR_TX_CLK	SoundWire transmit clock
K27	WCD_SWR_TX_DATA0	SoundWire transmit data 0
K28	WCD_SWR_TX_DATA1	SoundWire transmit data 1
K29	WCD_SWR_RX_CLK	SoundWire receive clock
K30	WCD_SWR_RX_DATA0	SoundWire receive data 0
K31	WCD_SWR_RX_DATA1	SoundWire receive data 1
K32	GPIO_0	GPIO 0
K33	GPIO_134	GPIO 134
K34	GPIO_133	GPIO 133
K35	GPIO_123	GPIO 123
K36	GPIO_26	GPIO 26
K37	CAM0_RST_N	Camera 0 reset, GPIO 93
K38	GPIO_6_PWM	PWM output, PM8150L GPIO 6
K39	DISPLAY_RESX2	GPIO 136
K40	RGB_1V2_EN	GPIO 115
K41[note1]	GPIO 116	See below table
K42[note1]	GPIO 70	See below table
K43	DMIC01_CLK	DMIC0/1 clock
K44	DMIC01_DATA	DMIC0/1 data
K45	BATT_ID	Battery ID
K46	BATT_THERM	Battery temperature sense
K47	VBAT_CON	VBAT
K48	VBAT_CON	VBAT
K49	VBAT_CON	VBAT
K50	VBAT_CON	VBAT

Note1: Below pins can be configured by GPIO 60 settings.

Pin	Signal Name	GPIO 60=L	GPIO 60=H
D38	GPIO_140_CON	GPIO 140	WL_XFEM_CTRL_LAA_TXEN_GPIO
E37	GPIO_145_CON	GPIO 145	WL_XFEM_CTRL_WL_TXEN_GPIO
K41	GPIO_116_CON	GPIO 116	LTE_COEX_TXD_GPIO
K42	GPIO_70_CON	GPIO 70	LTE_COEX_RXD_GPIO

3.2 J2 BTB Connector

Pin	Signal Name	Pin	Signal Name
1	SDM_JTAG_TMS	9	SDM _JTAG_SRST_N
2	SDM_JTAG_TCK	10	SDM _DEBUG_UART_TX
3	SDM _JTAG_TDO	11	SDM_DEBUG_UART_RX
4	SDM _JTAG_TDI	12	VREG_S4A_1P8
5	SDM _JTAG_TRST_N	13	SDM _PS_HOLD
6	DEBUG_PMIC_PKD_N	14	SDM _FORCE_USB_BOOT
7	DEBUG_KEY_VOL_DOWN_N	15	SDM _WDOG_DISABLE
8	GND	16	SDM _RESOUT_N

4 Electrical Characteristics

4.1 Absolute Maximum Ratings

The SOM needs to be designed in the operation conditions which is shown as below table.

Parameter	Min	Max	Units
Input Power Voltage			
USB_VBUS	-0.3	28	V
VBAT	-0.3	6	V
VBATT_CONN_VSENSE_P, VBATT_CONN_VSENSE_M, RSENSE_EXT_M, RSENSE_EXT_P	-0.3	6	V
ESD			
ESD-HBM model rating		±2000	V
ESD-CDM model rating		±500	V

Table 4.1-1 Absolute rating condition

Notes*: for the ESD, it will be valid and available only when the module is fully tested and approved in the Initial Production stage.*

4.2 Operating Conditions

The SOM needs to be designed in the operation conditons which is shown as below table.

Parameters	Min	Typical	Max	Units
Input Power voltage				
USB_VBUS	+3.6	5	+13.2	V
VBAT	+3.6	3.8	+4.8	V
VBAT	3			A
VBATT_CONN_VSENSE_P, VBATT_CONN_VSENSE_M, RSENSE_EXT_M, RSENSE_EXT_P	+3.6	3.8	+4.8	V
Thermal conditions				
Operating temperature	-20	25	70	°C
Storage temperature	-40	-	70	°C

Table 4.2-1 Operating condition

Note: *For the thermal conditons, operatin and storage min and max temperature is only when the module is fully tested and approved in the Initial Production stage.*

4.3 Output Power

The SOM provide power supply for external device, like camera module, SD card, Sensor, and so on. Below map show the details.

Function	Default voltage(V)	Programble range(V)	Rated current(mA)	Expected use
VREG_L11C_3P3	+3.104	+3.0-+3.312	600	
VREG_L9C_2P96	+2.96	+2.7--+2.96	600	SD/MMC card or UFS card
VREG_L5C_1P8	+1.808	+1.808	150	NFC-UICC2
VREG_L8C_1P8	+1.8	+1.8	150	LVS for sensor
VREG_IO_1P8	+1.8	TBD	TBD	SPMI
VREG_L2A_3P1	+3.072	+3.072	150mA	USB
VREG_S4A_1P8	+1.8	+1.8	3500	Generic 1.8V
VREG_BOB	+3.7	+3.6--+4.0	600	for Codec VDD input Each Pin is 300mA

Table 4.3-1 Output power

4.4 Digital-logic characteristics

The digital I/Os performance depe nds on its pad type, usage, and power supply voltage.The SOM IO voltage level is the same with VDDPX_3 except the SD card and analog input/output. The I2C, USB,MIPI and UART comply with the standards.

4.4.1 Digital GPIO characteristics

The follow-int table shows the digital GPIO characteristics:

Parameter	Description	Min	Max	Units
VIH	High-level input voltage, CMOS/Schmitt,	0.7 x VDDPX_3	VDDPX_3+0.3	V
VIL	Low-level input voltage, CMOS/Schmitt,	-0.3	0.3 x VDDPX_3	V
VSHYS	Schmitt hysteresis voltage	300	-	mV
VOH	High-level output voltage, CMOS	VDDPX_3 - 0.45	VDDPX_3	V

VOL	Low-level output voltage, CMOS	0.0	0.45	V
RPULL-UP	Pull-up resistance	20 K	60 K	Ω
RPULL-DOWN	Pull-down resistance	60 K	20 K	Ω

Table 4.4-1 Digital IO voltage performance

4.4.2 SD card digital I/O characteristics

The SD card is powered by P2 supply; the power is 1.8V and 2.96V.the following table shows the SD card digital I/O characteristics:

Parameter	Description	Min	Typical	Max	Units
VIH	High-level input voltage	1.27/0.625 x VDDPX_2	-	2/VDDPX_2 + 0.3	V
VIL	Low-level input voltage	-0.3/-0.3	-	0.58/0.25 x VDDPX_2	V
VHYS	Schmitt hysteresis voltage	100	-	-	mV
RPULL-UP	Pull-up resistance	10 K	-	100K	Ω
RPULL-DOWN	Pull-down resistance	10 K	-	100K	Ω
RKEEPER-UP	Keeper-up resistance	10 K	-	100K	Ω
RKEEPER-DOWN	Keeper-down resistance	10 K	-	100K	Ω
VOH	High-level output voltage	1.4/0.75 x VDDPX_2	-	-/VDDPX_2	V
VOL	Low-level output voltage	0/0	-	0.45/0.125 x VDDPX_2	V

Table 4.4-2 SD digital IO voltage performance (1.8V/2.96V)

4.5 MIPI

The SOM supports the MIPI interface and comply with MIPI standards.

Applicable standard	Feature exceptions
MIPI Alliance Specification for Display Serial Interface	None
MIPI Alliance Specification for DPHY v1.2	None

MIPI Alliance Specification for CPHY v1.0	None

Table 4.5-1 MIPI_DSI

Applicable standard	Feature exceptions
MIPI Alliance Specification for CSI-2 v1.3	RAW7 not supported DPCM predictor 2 not supported
MIPI Alliance Specification for DPHY v1.2	None
MIPI Alliance Specification for CPHY v1.0	The maximum supported data rate is 1.5Gsps

Table 4.5-2 MIPI_CSI

4.6 USB

The SOM supports USB standards and exceptions.

Applicable standard	Feature exceptions
Universal Serial Bus Specification, Revision 3.1 (August 11, 2014 or later)	SS Gen 2
UTMI Specification Version 1.05, released on 3/29/2001	None
On-The-Go and Embedded Host Supplement to the USB 3.0 Specification (May 10, 2012, Revision 1.1 or later)	None

Table 4.6-1 USB

4.7 PCIe

The SOM supports PCIe standards and exceptions

Applicable standard	Feature exceptions
PCI Express Specification, Revision 3.0	Gen3

Table 4.7-1 PCIe

4.8 DisplayPort

The SOM supports DisplayPort standards and exceptions

Applicable standard	Feature exceptions

VESA DisplayPort V1.4	HBR3

Table 4.8-1 DP

4.9 SLIMbus

The SOM supports SLIMbus HDMI standards and exceptions

Applicable standard	Feature exceptions
MIPI Alliance Specification for Serial Low-power Interchip Media Bus Version 1.01.01	None

Table 4.9-1 SLIMbus

4.10 SDIO

The SOM Supports SD standards and exceptions

Applicable standard	Feature exceptions
Secure Digital: Physical Layer Specification version 3.0	None
SDIO Card Specification version 3.0	None

Table 4.10-1 SDIO

4.11 I2S

The SOM I2S standards and exceptions:

- Legacy I2S interfaces for primary and secondary microphones and speakers.
- The multiple I2S (MI2S) interface for microphone and speaker functions.

It is supports both master and slave mode.
Supports 16, 24, or 32-bit resolution audio samples
Supports 8, 16, 32, 48, 96 and192 kHz sampling rate in Master mode, and all standard sample rates in Slave mode. Supports 16-bit and 24-bit data formats in standard I2S mode, and 24-bit left-justified (24-bit data in 32-bit frame left-justified, LSBs are padded with 0s).
Maximum clock frequency supported 12.288 MHz.
An additional pin can be used for a master clock, supplied by the MSM device, the master clock is often used in the external devices to drive their oversampling logic. The LPASS clock controller can provide master clocks from independent clock dividers to the I2S bit-clock dividers.

Applicable standard	Feature exceptions
Philips I2S Bus Specifications revised June 5, 1996	None

Table 4.11-1 I2S

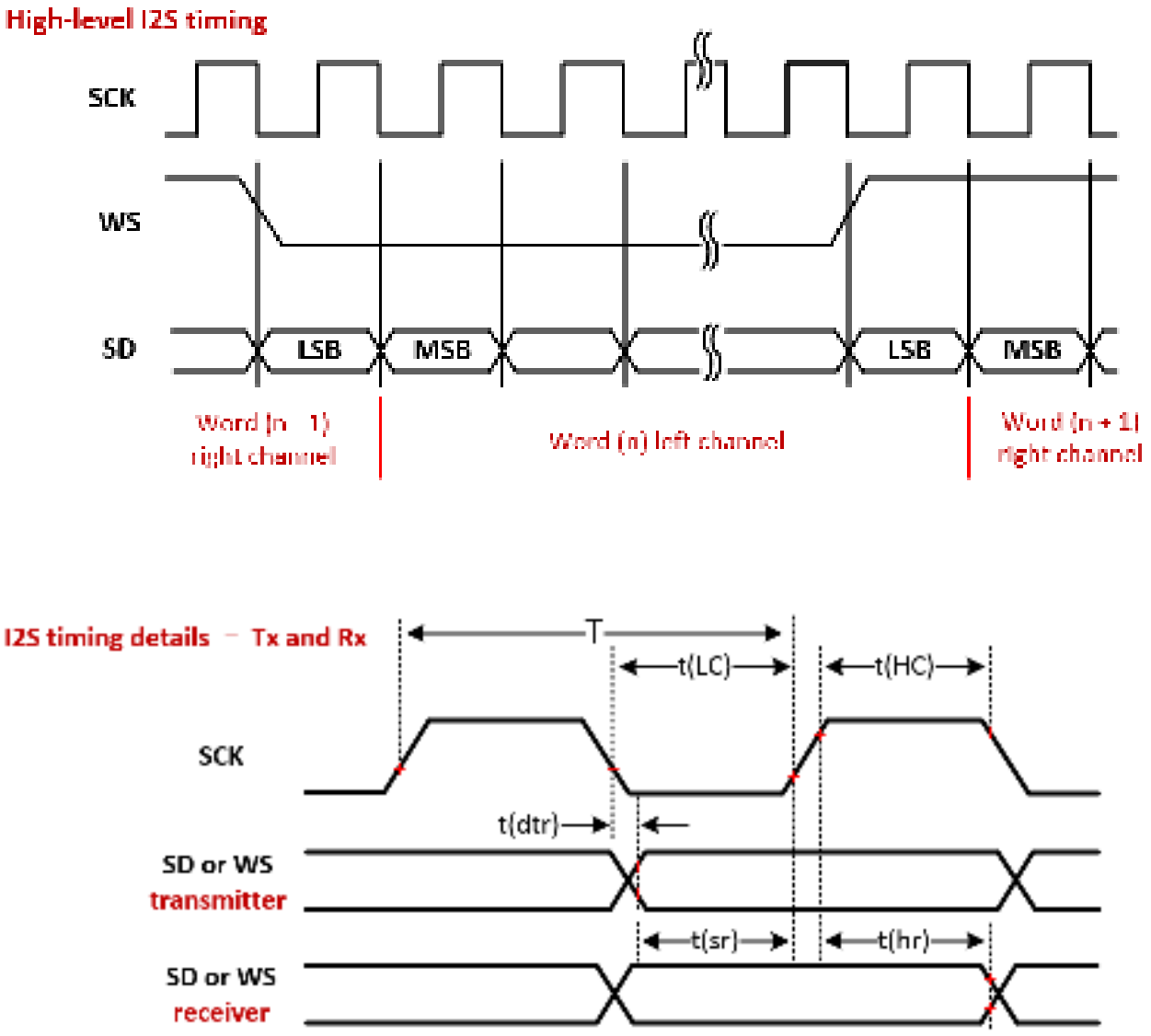

Figure 4.11-1 I2S timing diagram

The word-select signal is a 50% duty cycle signal Data is delayed 1 bit-clock, relative to the word select. Data outputs are launched on the falling edge of the clock, and inputs data are captured on the rising edge of the clock by the receiver.
I2S samples are 2's complement values, and the MSB is transmitted first allowing the transmitter and receiver to support different number of bits per sample.
The left channel is transmitted when the word select is low, and the right channel is transmitted when the word select is high

Parameter	Comments	Min	Typ	Max	Unit

Using internal SCK						
Frequency		–	–	–	24.576	MHz
T	Clock period	–	40.69	–	–	ns
t(HC)	Clock high	–	0.45 × T	–	0.55 × T	ns
t(LC)	Clock low	–	0.45 × T	–	0.55 × T	ns
t(sr)	SD and WS input setup time	–	8.14	–	–	ns
t(hr)	SD and WS input hold time	–	0	–	–	ns
t(dtr)	SD and WS output delay	–	–	–	6.10	ns
Using external SCK						
Frequency		–	–	–	24.576	MHz
T	Clock period	–	40.69	–	–	ns
t(HC)	Clock high	–	0.45 × T	–	0.55 × T	ns
t(LC)	Clock low	–	0.45 × T	–	0.55 × T	ns
t(sr)	SD and WS input setup time	–	8.14	–	–	ns
t(hr)	SD and WS input hold time	–	0	–	–	ns
t(dtr)	SD and WS output delay	–	–	–	6.10	ns

Table 4.11-2 I2S Timing

4.12 I2C

The SOM I2C standards and exceptions:

Applicable standard	Feature exceptions
I2C Specification, version 3.0	HS mode, slave mode, multi-master mode, and 10-bit addressing are not supported.

Table 4.12-1 I2C

4.13 SPI

The SOM supports **SPI** standards as a master only.

4.14 Fuel gauge

The fuel gauge module offers a hardware-based algorithm that is able to accurately estimate the Battery's state of charge by using current monitoring and voltage-based techniques. This hybrid approach ensures both excellent short-term linearity and long-term accuracy. Furthermore, neither full battery charge cycling, nor zero-current-load conditions, are required to maintain the accuracy.

The fuel gauge measures the battery pack temperature by sensing the voltage across an external thermistor. Missing battery detection is also incorporated to accurately monitor battery insertion and removal scenarios, while properly updating the state of charge when a battery is reconnected.

Using precise measurements of battery voltage, current, and temperature, the fuel gauging algorithm

compensates for the variation in battery characteristics across temperature changes and aging effects. This provides a dependable state of charge estimate throughout the entire life of the battery and across a broad range of operating conditions.

Function	Min	Type	Max	Units	Expected use
VBATT_CONN_VSENSE_P (H47)& VBATT_CONN_VSENSE_M(G47)					
Resolution			16	bits	Voltage ADC
	1		450	Kohm	ID ADC
			16	bits	Current ADC

Table 4.14-1 Fuel Gauge

4.15 LED Current Driver

Red, Green, and Blue (RGB) drivers, which operate off a dedicated supply voltage, are available.

Function	Min	Type	Max	Units	Expected use
RGB_LED					
Current per channel (I out)			12	mA	
Dimming PWM frequency	0.0025		4700	Hz	
Dimming Resolution	6		9	bit	

Table 4.15-1 LED current Driver

4.16 ADC

ADC performance specifications are listed in Table 4.16-1

Specification	Test condition	Min	Typ.	Max	Units	Expected use
1/1 channel end-to-end accuracy	Calibrated data result	-11	±6	11	mV	
1/1 channel end-to-end accuracy with internal pull-up	Calibrated data result	-12.5	±7	12.5	mV	
1/3 channel end-to-end accuracy	Calibrated data result	-20	±10	20	mV	
ADC resolution (LSB)	1/1 channel	-	64.879	-	µV	
	Scaled to 1/3 channel	-	194.637	-		
ADC conversion time	1K decimation ratio, 4.8MHz sample clock	-	654	700	µs	
Current consumption	VADC active	-	450	500	µA	

Table 4.16-1 ADC

4.17 Power Consumption

Power Consumption				
S/N	**Test Items and Test Condition**		UNIT	**DUT**
				average value
1	**Normal Operation Current (Play Movie)** -Play mp4 4K -Loudspeaker	4K60	mA	TBD
		1080P		TBD
2	**Normal Operation Current (Camera mode)** **-** HDMI Output	Take photo	mA	TBD
		video	mA	TBD
3	**Normal Operation Current (Sleep Mode)** - No LCD. No camera	WiFi ON	mA	TBD
		WiFi OFF	mA	TBD
4	**Leakage current**	-	μA	TBD

Table 4.17-1 Power Consumption

4.18 Thermal

This chart records thermal test data, to make sure the SOM working on high performance, strong suggest make solution for heat sink. Table 4.18-1 describes SOM thermal test point.

Thermal Test Condition		
1	Test case	The test script of CPU + HDMI Out + WiFi/BT open + Play Game
2	HW Version	TurboX-C865 SOM-V02
3	Test points	CPU +LPDDR5 UFS , PM8250, PM8150B, PM8150L, QCA6391
4	Ambient temperature	25℃

Table 4.18-1 Thermal Test

Thermal Test Result			
	Test Location	Temperature(Max)	△T
1	Environment Temperature	25	
2	DDR	TBD	TBD
3	UFS	TBD	TBD
4	PM8250	TBD	TBD
5	PM8150B	TBD	TBD
6	PM8150L	TBD	TBD
7	QCA6391	TBD	TBD
8	PCB	TBD	TBD

Figure 4.18-1 Thermal Data Heat Sink Design