SARA-S520BM10

Multimode LTE-M / Satellite / GNSS module

System integration manual

Abstract

This document describes the features and the guidelines for the integration of SARA-S520BM10 multimode modules, offering connectivity on both the LTE-M cellular terrestrial networks and the ORBCOMM satellite network and with the latest u-blox UBX-R52 chipset, as well as accurate and reliable GNSS positioning capability with the u-blox's leading M10 GNSS receiver, in the very small and compact SARA form factor.

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This document applies to the following products:

Product name	Type number
SARA-S520BM10	SARA-S520BM10-00B-00

For firmware version, notification document, and product status, see the data sheet [1].

Contents

1 System description

1.1 Overview

The SARA-S520BM10 module, powered by the latest u-blox UBX-R52 Cellular / Satellite chipset and the u-blox's leading M10 GNSS receiver chipset, offers comprehensive connectivity capabilities, including access to LTE-M Cellular terrestrial networks and access to the IsatData Pro (IDP) Satellite service provided by ORBCOMM, in the miniature SARA LGA form factor (26.0 x 16.0 mm, 96-pin).

With complete hardware and software ownership, u-blox ensures long-term device availability and lifetime support at the chipset level. The miniature SARA form factor allows easy integration into compact designs and a seamless drop-in migration from other u-blox cellular module families.

Designed for applications requiring constant network connectivity worldwide, the SARA-S520BM10 module leverages GEO satellite network ecosystem to ensure seamless coverage across the globe, using the IsatData Pro (IDP) fully reliable protocol designed for IoT solutions provided by ORBCOMM.

On top of the Satellite connectivity, SARA-S520BM10 modules support LTE-M Cellular connectivity optimized for IoT applications, boasting enhancements in power consumption, coverage, data rate, and mobility.

Moreover, the SARA-S520BM10 modules integrate the u-blox M10 GNSS receiver chipset to deliver best-in-class positioning data concurrently with the LTE-M Cellular connectivity, making it the ideal solution for continuous or cyclic tracking applications.

Cellular LTE-M connectivity and Satellite IDP connectivity can be alternatively enabled, in a mutually exclusive way. GNSS signals reception can be concurrently available during Cellular LTE-M signals transmission and reception, and during Satellite IDP signals reception.

SARA-S520BM10 modules are compatible with other u-blox cellular modules in SARA form-factor, as well as compatible with u-blox cellular module families in LARA, LENA, LISA and TOBY form-factors, facilitating migration from u-blox cellular modules supporting various radio access technologies, maximizes customer investments, simplifies logistics, and enables very short time-to-market.

Table 1 lists the main features and interfaces of SARA-S520BM10 modules.

Model	Region	Radio Access Technology						GNSS		u-blox Services			External Interfaces				Features															Grade		
		LTE 3GPP category	LTE bands	LTE power class [dBm]	Satellite protocol	Satellite band	Satellite power class [dBm]	Integrated GNSS receiver	Dedicated GNSS / Satellite antenna interface	AssistNow™	CellLocate®	CloudLocate	UARTs	USB (for diagnostics)	I2C	USIM	GPIOs	u-blox open CPU solution (uCPU)	Secure boot, updates	Antenna dynamic tuning	Ultra-low consumption in PSM / eDRX	Embedded TCP/UDP	Embedded HTTP, FTP	Embedded TLS, DTLS	Embedded MQTT, MQTT-SN	Embedded COAP and LwM2M	FW update via serial (FOAT)	u-blox FW update Over the Air (uFOTA)	Last gasp	Jamming detection	Antenna and SIM detection	CellTime	Standard	Professional	Automotive
SARA-S520BM10	Global	M1	1,2,3,4,58, 12,13 18,19,20 25,26,28 66,71,85	23	IDP	L	31.5	•	•	•	•	•	•	•	•	•	•	•	•	•	•	•	•	•	•	•	•	•	•	•	•		•	

Table 1: SARA-S520BM10 main features summary

Table 2 summarizes cellular and GNSS characteristics of the modules.

Item	SARA-S520BM10
Cellular protocol	Including key 3GPP Release14 features for LTE Cat M1
Cellular data rate	LTE category M1 Half-duplex: up to 1200 kbit/s UL, up to 588 kbit/s DL
Cellular power class	LTE power class 3 (23 dBm)
Cellular operating bands	Band 1 (2100 MHz) Band 2 (1900 MHz) Band 3 (1800 MHz) Band 4 (1700 MHz) Band 5 (850 MHz) Band 8 (900 MHz) Band 12 (700 MHz) Band 13 (750 MHz) Band 18 (850 MHz) Band 19 (850 MHz) Band 20 (800 MHz) Band 25 (1900 MHz) Band 26 (850 MHz) Band 28 (700 MHz) Band 66 (1700 MHz) Band 71 (600 MHz) Band 85 (700 MHz)
Satellite protocol	IsatData Pro (IDP)
Satellite max payload	6.4 kbytes UL, 10.0 kbytes DL
Satellite power class	31.5 dBm
Satellite operating bands	Transmit frequency bands: 1626.5-1660.5 MHz Receive frequency bands: 1525-1559 MHz
GNSS receiver type	u-blox M10050 SPG 5.10 receiver supporting concurrent reception of up to four GNSS systems GPS / QZSS L1C/A, Galileo E1-B/C, GLONASS L1OF, BeiDou B1I, BeiDou B1C, SBAS (EGNOS, GAGAN, MSAS and WAAS), QZSS L1S (SLAS)

Table 2: SARA-S520BM10 modules cellular, satellite and GNSS characteristics summary

1.2 Architecture

Figure 1 summarizes the internal architecture of SARA-S520BM10.

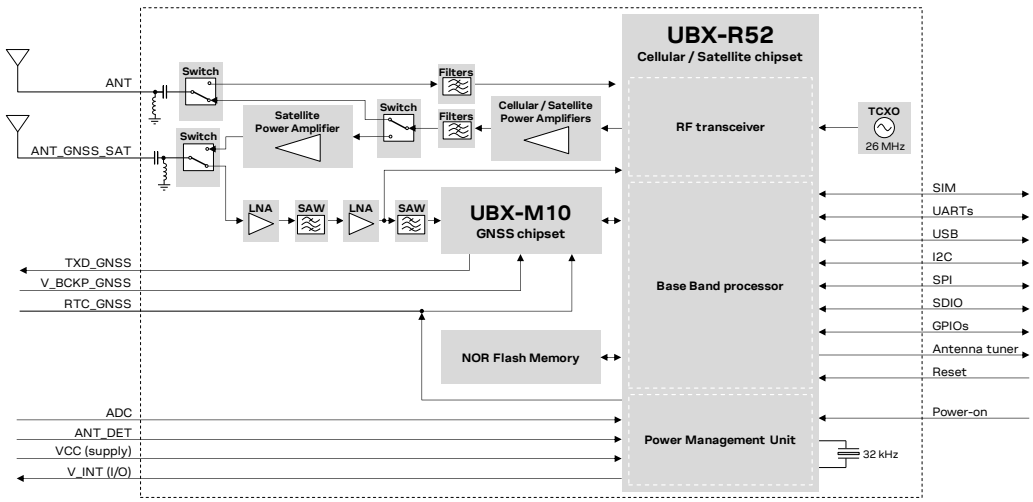

Figure 1: SARA-S520BM10 module simplified block diagram

The current products version of the SARA-S520BM10 modules do not support SPI and SDIO interfaces. They should be left unconnected and should not be driven by external devices.

SARA-S520BM10 modules internally consist of the following sections, described with more details than the simplified block diagrams of Figure 1.

RF section

Composed of the following main elements:

- RF switch connecting the Cellular antenna port (**ANT**) to the suitable internal RF Tx / Rx paths for LTE Cat M1 Half-Duplex operations
- RF switch connecting the GNSS / Satellite antenna port (**ANT_GNSS_SAT**) to the internal RF Tx path from the Satellite Power Amplifier, or to the internal Rx paths up to both the Satellite receiver integrated in the UBX-R52 chipset and up to the GNSS receiver consisting in the UBX-M10 chipset.
- Power Amplifiers amplifying the Cellular / Satellite Tx signal modulated and pre-amplified by the RF transceiver integrated in the UBX-R52 chipset
- Power Amplifier amplifying the Satellite Tx signal pre-amplified by the Power Amplifier above
- RF switch to direct the Tx signal either to the Satellite Tx path or the Cellular Tx path
- RF filters along the Tx and Rx signal paths providing RF filtering
- Two series Low Noise Amplifier (LNA) and GNSS / Satellite pass-band SAW filter along the GNSS / Satellite receiver RF Rx path, plus one additional GNSS pass-band SAW filter along the GNSS receiver RF Rx path
- RF transceiver integrated in the u-blox UBX-R52 Cellular / Satellite chipset, performing modulation, up-conversion and pre-amplification of the baseband signals for both Cellular and Satellite RF signals transmission, and performing down-conversion and demodulation of RF signals for both Cellular and Satellite signals reception
- 26 MHz Temperature-Controlled Crystal Oscillator (TCXO) generating the reference clock signal for the RF transceiver, the baseband system and the GNSS system, when the related system is in active mode or connected mode

Baseband and power management section

Based on the latest u-blox UBX-R52 cellular chipset, and composed of the following main elements:

- On-chip modem processor, vector signal processor, with dedicated hardware assistance for signal processing and system timing
- On-chip modem processor, with interfaces control functions
- On-chip voltage regulators to derive all the internal or external (**V_SIM**, **V_INT**) supply voltages from the module supply input **VCC**
- On-chip cryptographic hardware acceleration with Root of Trust
- On-chip memory system, including PSRAM and secure boot ROM
- Dedicated flash memory IC
- 32.768 kHz crystal oscillator to provide the clock reference in the low power idle mode, which can be enabled using the +UPSV AT command, and in the PSM / eDRX deep-sleep mode

GNSS section

Based on the u-blox UBX-M10 GNSS chipset, with the following main elements illustrated in Figure 2:

- RF switch connecting the GNSS / Satellite antenna port (**ANT_GNSS_SAT**) to the internal GNSS receiver / Satellite receiver RF Rx path, or to the Satellite Power Amplifier RF Tx path
- Low Noise Amplifier (LNA) along the GNSS receiver / Satellite receiver RF Rx path
- GNSS / Satellite pass-band SAW filter along the GNSS receiver / Satellite receiver RF Rx path
- Low Noise Amplifier (LNA) along the GNSS receiver / Satellite receiver RF Rx path
- GNSS pass-band SAW filter along the GNSS receiver RF Rx path
- u-blox UBX-M10050 concurrent GNSS chipset with SPG 5.10 firmware version
- 26 MHz Temperature-Controlled Crystal Oscillator (TCXO) generating the reference clock signal for the cellular RF transceiver, the baseband system and the GNSS system

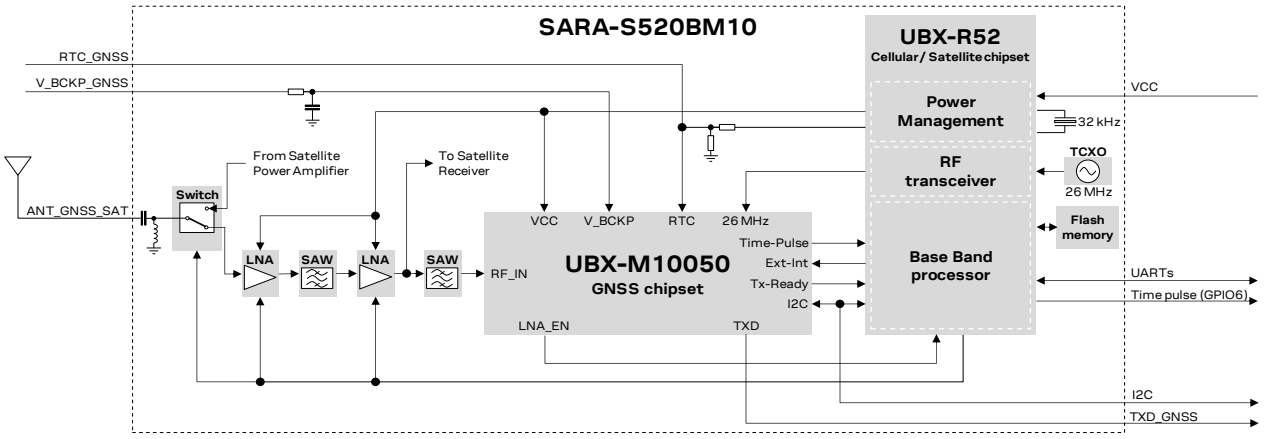

Figure 2: SARA-S520BM10 modules GNSS section block diagram

1.3 Pin-out

Table 3 lists the pin-out of the SARA-S520BM10 modules, with pins grouped by function.

Function	Pin name	Pin no.	I/O	Description	Remarks
Power	VCC	51,52,53	I	Module supply input	VCC supply circuit affects the RF performance and compliance of the device integrating the module with applicable required certification schemes. See section 1.5.1 for description and requirements. See section 2.2.1 for external circuit design-in.
	GND	1,3,5,14,20 22,30,32, 43,50,54, 55,57-61, 63-96	N/A	Ground	GND pins are internally connected to each other. External ground connection affects the RF and thermal performance of the device. See section 1.5.1for functional description. See section 2.2.1 for external circuit design-in.
	V_INT	4	O	Generic digital interfaces supply output	1.8 V (typ.) generated by internal regulator with the module switched on, outside low power deep-sleep mode. See section 1.5.2 for functional description. See section 2.2.2 for external circuit design-in. Provide test point for diagnostic purposes.
	V_BCKP_GNSS	2	I	GNSS backup voltage supply	Integrates 10R series resistor and 2.2µF shunt capacitor. See section 1.5.3 for functional description. See section 2.2.3 for external circuit design-in.
System	PWR_ON	15	I	Power-on / power-off input	Internal active pull-up. Active low. See sections 1.6.1, 1.6.2 for functional description. See section 2.3.1 for external circuit design-in. Provide test point for diagnostic purposes.
	RESET_N	18	I	External reset input	Internal active pull-up. Active low. See section 1.6.2.3 for functional description. See section 2.3.2 for external circuit design-in. Provide test point for diagnostic purposes.
Antenna	ANT	56	I/O	Cellular antenna	50 Ω nominal characteristic impedance. Antenna circuit affects RF performance and application device compliance with required certification schemes. See section 1.7.1 for description and requirements. See section 2.4.2 for external circuit design-in.
	ANT_GNSS_SAT	31	I/O	GNSS / Satellite antenna	50 Ω nominal characteristic impedance. See section 1.7.2 for description and requirements. See section 2.4.3 for external circuit design-in.
	ANT_DET	62	I	Antenna detection	ADC for antenna presence detection function. See section 1.7.3 for functional description. See section 2.4.5 for external circuit design-in.

Function	Pin name	Pin no.	I/O	Description	Remarks
SIM	VSIM	41	O	SIM supply output	VSIM = 1.8 V / 3 V output as per the connected SIM type. See section 1.8 for functional description. See section 2.5 for external circuit design-in.
	SIM_IO	39	I/O	SIM data	Data input/output for 1.8 V / 3 V SIM. Internal pull-up to VSIM. See section 1.8 for functional description. See section 2.5 for external circuit design-in.
	SIM_CLK	38	O	SIM clock	Clock output for 1.8 V / 3 V SIM. See section 1.8 for functional description. See section 2.5 for external circuit design-in.
	SIM_RST	40	O	SIM reset	Reset output for 1.8 V / 3 V SIM. See section 1.8 for functional description. See section 2.5 for external circuit design-in.
UART	RXD	13	O	UART data output	USIO variants 0 / 1 / 2 / 3 / 4: Primary UART circuit 104 (RxD) in ITU V.24, for AT, data, Mux, FOAT, FW update via EasyFlash. See section 1.9.1 for functional description. See section 2.6.1 for external circuit design-in. Provide test point for FW update purposes.
	TXD	12	I	UART data input	USIO variants 0 / 1 / 2 / 3 / 4: Primary UART circuit 103 (TxD) in ITU V.24, for AT, data, Mux, FOAT, FW update via EasyFlash. Internal active pull-up enabled. See section 1.9.1 for functional description. See section 2.6.1 for external circuit design-in. Provide test point for FW update purposes.
	CTS	11	O	UART clear to send output	USIO variants 0 / 1 / 2 / 3 / 4: Primary UART circuit 106 (CTS) in ITU V.24. See section 1.9.1 for functional description. See section 2.6.1 for external circuit design-in.
	RTS	10	I	UART request to send input	USIO variants 0 / 1 / 2 / 3 / 4: Primary UART circuit 105 (RTS) in ITU V.24. Internal active pull-up enabled. See section 1.9.1 for functional description. See section 2.6.1 for external circuit design-in.
	DSR	6	O / I	UART data set ready output / AUX UART request to send input	USIO variant 0: Pin disabled USIO variant 1: Primary UART circuit 107 (DSR) in ITU V.24. USIO variants 2 / 3 / 4: Auxiliary UART circuit 105 (RTS) in ITU V.24. Internal active pull-up enabled. See section 1.9.1 for functional description. See section 2.6.1 for external circuit design-in.
	RI	7	O / O	UART ring indicator output / AUX UART clear to send output	USIO variants 0 / 1: Primary UART circuit 125 (RI) in ITU V.24. USIO variants 2 / 3 / 4: Auxiliary UART circuit 106 (CTS) in ITU V.24. See section 1.9.1 for functional description. See section 2.6.1 for external circuit design-in.

Function	Pin name	Pin no.	I/O	Description	Remarks
	DTR	9	I / I	UART data terminal ready input / AUX UART data input	USIO variants 0 / 1: Primary UART circuit 108/2 (DTR) in ITU V.24. Internal active pull-up enabled. USIO variants 2 / 3 / 4: Auxiliary UART circuit 103 (TxD) in ITU V.24, for AT, data, GNSS tunneling, FOAT, diagnostics. Internal active pull-up enabled. See section 1.9.1 for functional description. See section 2.6.1 for external circuit design-in. Provide test point for diagnostic purposes.
	DCD	8	O / O	UART data carrier detect output / AUX UART data output	USIO variant 0: Pin disabled. USIO variant 1: Primary UART circuit 109 (DCD) in ITU V.24. USIO variants 2 / 3 / 4: Auxiliary UART circuit 104 (RxD) in ITU V.24, for AT, data, GNSS tunneling, FOAT, diagnostics. See section 1.9.1 for functional description. See section 2.6.1 for external circuit design-in. Provide test point for diagnostic purposes.
USB	VUSB_DET	17	I	USB detect input	VBUS (5 V typical) must be connected to this input pin to enable the USB interface. See section 1.9.2 for functional description. See section 2.6.2 for external circuit design-in. Provide test point for diagnostic purposes, with 10 Ohm series resistor (0402 or similar) to avoid exceeding the absolute maximum rating for voltage ramp.
	USB_D-	28	I/O	USB Data Line D-	USB interface for diagnostics. See section 1.9.2 for functional description. See section 2.6.2 for external circuit design-in. Provide test point for diagnostic purposes.
	USB_D+	29	I/O	USB Data Line D+	USB interface for diagnostics. See section 1.9.2 for functional description. See section 2.6.2 for external circuit design-in. Provide test point for diagnostic purposes.
SPI	SDIO_D0	47	O	SPI data output	SPI data output, supported for diagnostics only.
	SDIO_D1	49	I	SPI data input	SPI data input, supported for diagnostics only.
	SDIO_D2	44	O	SPI clock	SPI clock, supported for diagnostics only.
	SDIO_D3	48	O	SPI Chip Select	SPI chip selectsupported for diagnostics only.
SDIO	SDIO_D0	47	I/O	SDIO serial data [0]	Alternatively configurable as SPI. SDIO not supported.
	SDIO_D1	49	I/O	SDIO serial data [1]	Alternatively configurable as SPI. SDIO not supported.
	SDIO_D2	44	I/O	SDIO serial data [2]	Alternatively configurable as SPI. SDIO not supported.
	SDIO_D3	48	I/O	SDIO serial data [3]	Alternatively configurable as SPI. SDIO not supported.
	SDIO_CLK	45	O	SDIO serial clock	SDIO not supported.
	SDIO_CMD	46	I/O	SDIO command	Alternatively configurable by +UGPIOC AT command. SDIO not supported.

Function	Pin name	Pin no.	I/O	Description	Remarks
I2C	SCL	27	O	I2C bus clock line	Fixed open drain, for communication with I2C devices. Internal active pull-up. See section 1.9.5 for functional description. See section 2.6.5 for external circuit design-in.
	SDA	26	I/O	I2C bus data line	Fixed open drain, for communication with I2C devices. Internal active pull-up. See section 1.9.5 for functional description. See section 2.6.5 for external circuit design-in.
ADC	ADC	21	I	ADC input	See section 1.10 for functional description. See section 2.7 for external circuit design-in.
GPIO	GPIO1	16	I/O	GPIO	Pin with alternatively configurable functions. See section 1.11 for functional description. See section 2.8 for external circuit design-in.
	GPIO2	23	I/O	GPIO	Pin with alternatively configurable functions. See section 1.11 for functional description. See section 2.8 for external circuit design-in.
	GPIO3	24	I/O	GPIO	Pin with alternatively configurable functions. See section 1.11 for functional description. See section 2.8 for external circuit design-in.
	GPIO4	25	I/O	GPIO	Pin with alternatively configurable functions. See section 1.11 for functional description. See section 2.8 for external circuit design-in.
	GPIO5	42	I/O	GPIO	Pin with alternatively configurable functions. See sections 1.8.2 and 1.11 for description. See sections 2.5 and 2.8 for circuit design-in.
	GPIO6	19	I/O	GPIO	Pin with alternatively configurable functions. See section 1.11 for functional description. See section 2.8 for external circuit design-in.
	GPIO7	37	I/O	GPIO	Pin with alternatively configurable functions. See section 1.11 for functional description. See section 2.8 for external circuit design-in.
Antenna tuning	RFCTRL1	34	O	RF GPIO for cellular antenna tuning	Optional output for antenna dynamic tuning. See section 1.12 for functional description. See section 2.4.6 for functional description / design-in.
	RFCTRL2	35	O	RF GPIO for cellular antenna tuning	Optional output for antenna dynamic tuning. See section 1.12 for functional description. See section 2.4.6 for functional description / design-in.
GNSS PIO	TXD_GNSS	36	O	GNSS data output	GNSS UART data output from internal u-blox M10 chip. See section 1.13 for functional description. See section 2.9 for external circuit design-in.
GNSS RTC	RTC_GNSS	33	I	GNSS RTC input	Oscillator input for 32.768 kHz clock. See section 1.14 for functional description. See section 2.10 for external circuit design-in. Leave unconnected if not used or if RTC clock is generated internally.

Table 3: SARA-S520BM10 modules pin definition, grouped by function

1.4 Operating modes

SARA-S520BM10 modules have several operating modes as defined in Table 4.

Status	Operating Mode	Definition
Power-down	**Not-powered mode**	**VCC** supply not present or below operating range: module is switched off.
	Power-off mode	**VCC** supply within operating range and module is switched off.
Normal operation	**Deep-sleep mode**	RTC runs with 32 kHz reference internally generated.
	Idle mode	Module processor runs with 32 kHz reference internally generated.
	Active mode	Module processor runs with 26 MHz reference internally generated.
	Connected mode	RF Tx/Rx data connection enabled and processor core runs with 26 MHz reference.

Table 4: SARA-S520BM10 modules operating modes definition

Figure 3 describes the transition between the different operating modes.

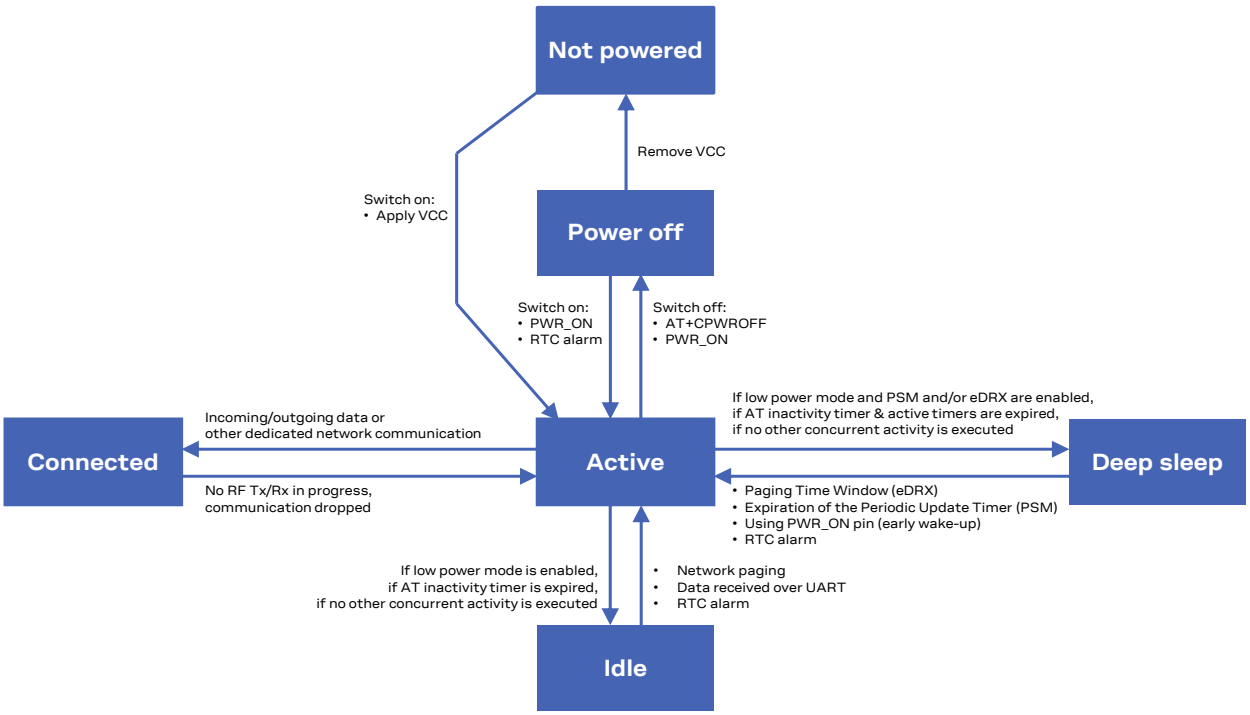

Figure 3: SARA-S520BM10 modules operating modes transitions

The initial operating mode of SARA-S520BM10 modules is the not-powered mode: **VCC** supply is not present or below the operating range. The modules are switched off.

Once a valid **VCC** supply is applied to the SARA-S520BM10 modules, the switch-on routine of the modules is triggered, and the modules enter the active mode.

SARA-S520BM10 modules are ready to operate when in active mode: the available communication interfaces are completely functional and the modules can accept and respond to any AT command, entering connected mode upon LTE / Satellite signal reception / transmission.

Cellular LTE mode, with LTE signal reception / transmission, and Satellite mode, with Satellite signal reception / transmission, can be alternatively enabled, in mutually exclusive way.

The internal GNSS functionality can be enabled by the +UGPS AT command, so that the internal GNSS receiver can operate concurrently with cellular LTE Tx/Rx operations, concurrently with Satellite Rx operations and in time-sharing with Satellite Tx operations.

If the low power configuration is enabled by the +UPSV AT command, the SARA-S520BM10 modules switch from active mode to the low power idle mode whenever possible.

The low power idle mode can last different time periods according to the specific +UPSV AT command setting, according to the specific +CEDRXS / +CEDRXRDP AT commands setting, and according to the concurrent activities executed by the module. For eDRX sleep time longer than 70 s, the modules can enter the ultra-low power eDRX deep-sleep mode, out of the Paging Time Window (PTW). Then, according to the +CPSMS / +UCPSMS AT commands setting, and according to the concurrent activities executed by the module, whenever possible, the modules can enter the ultra-low power PSM deep-sleep mode.

Once the modules enter the ultra-low power PSM / eDRX deep-sleep mode, the communication interfaces are not functional: the expiration of the “Periodic Update Timer” negotiated with the LTE network (for PSM cycles), the PTW occurrence (for eDRX cycles) or an early wake-up event, consisting in proper toggling of the **PWR_ON** input line, is necessary to trigger the wake-up routine of the modules that subsequently enter back into the active mode.

SARA-S520BM10 modules can be gracefully switched off by the +CPWROFF AT command, or by proper toggling of the **PWR_ON** input.

☞ See the AT commands manual [2] for possible configurations and settings of different operating modes.

1.5 Supply interfaces

1.5.1 Module supply input (VCC)

The modules must be supplied via the three **VCC** pins that represent the module power supply input.

Voltage must be stable, because during operation, the current drawn by the SARA-S520BM10 modules through the **VCC** pins may vary significantly, depending on the operating mode and state (as described in sections 1.5.1.2, 1.5.1.3, 1.5.1.4, 1.5.1.5 and 1.5.1.6).

It is important that the supply source can withstand the average current consumption occurring during satellite Tx at maximum RF power level (see the SARA-S520BM10 data sheet [1]).

The 3 **VCC** pins of SARA-S520BM10 modules are internally connected each other to both the internal power amplifier and the internal baseband power management unit.

Figure 4 provides a simplified block diagram of the SARA-S520BM10 modules’ internal VCC supply routing.

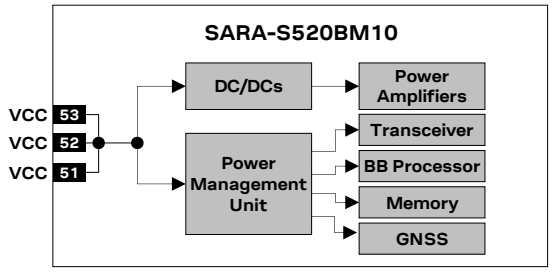

Figure 4: SARA-S520BM10 modules’ illustrative internal VCC supply routing

1.5.1.1 VCC supply requirements

Table 5 summarizes the requirements for the VCC modules supply. See section 2.2.1 for suggestions to correctly design a **VCC** supply circuit compliant with the requirements listed in Table 5.

⚠ The supply circuit affects the RF compliance of the device integrating SARA-S520BM10 modules with applicable required certification schemes as well as antenna circuit design. RF performance is optimized by fulfilling the requirements summarized in the Table 5.

Item	Requirement	Remark
VCC nominal voltage	Within **VCC** normal operating range: 3.3 V / 4.4 V	Operating within 3GPP / ETSI specifications: RF performance is optimized when **VCC** PA voltage is inside the normal operating range limits.
VCC voltage during normal operation	Within **VCC** extended operating range: 3.0 V / 4.5 V	Operating with possible slight deviation in RF performance outside normal operating range. **VCC** voltage must be above the extended operating range minimum limit to switch-on the module and to avoid possible switch-off of the module. Operation above **VCC** extended operating range is not recommended and may affect device reliability.
VCC current	Support with adequate margin the highest **VCC** current consumption value during Tx conditions specified in the SARA-S520BM10 data sheet [1]	The maximum current consumption can be greater than the specified value according to the actual antenna mismatching, temperature and supply voltage. For a safe design margin, use a VCC supply source that can deliver with adequate margin the maximum average VCC current consumption in Satellite connected mode, normal ambient temperature and normal voltage condition shown in the SARA-S520BM10 data sheet [1].
VCC voltage ripple	Noise in the supply pins must be minimized	High supply voltage ripple values during RF transmissions in connected mode directly affect the RF compliance with the applicable certification schemes.

Table 5: Summary of VCC modules supply requirements

1.5.1.2 VCC current consumption in Satellite connected mode

During a Satellite connection, SARA-S520BM10 modules transmit and receive in half duplex mode.

The current consumption during transmission depends on the output RF power, which is always set at roughly +31.5 dBm, according to ORBCOMM Satellite system specifications.

Transmissions fit within the same five-second subframe block structure used for reception and each block is divided into 10 subframes of 0.5 seconds each. Within the subframe block, the module may transmit in any of the subframes, except while the module is receiving, and the transmission may last up to 40 % of the subframes (up to 2 seconds).

It is important that the system power supply circuit can withstand with adequate safe design margin the maximum required current during transmission to the ORBCOMM Satellite system, even considering the transmission may last quite long.

The current consumption during reception is much less significant in magnitude as compared to the one during transmission.

For detailed consumption values, see SARA-S520BM10 data sheet [1].

1.5.1.3 VCC current consumption in LTE connected mode

During an LTE connection, the SARA-S520BM10 module transmit and receive in half duplex mode.

The current consumption during transmission depends on the output RF power, which may vary from less than -40 dBm up to roughly +23 dBm, as it is always regulated by the cellular network (the current base station), according to 3GPP specifications.

The transmission usually lasts quite a short time, but it may last differently depending on the amount of data to be transmitted and depending on the scheduling in use according to 3GPP specifications.

The current consumption during reception is much less significant in magnitude as compared to the one during transmission.

For detailed consumption values, see SARA-S520BM10 data sheet [1].

1.5.1.4 VCC consumption in active mode

The active mode is the state where the module is switched on and ready to communicate with an external device by the application interfaces (as the UART serial interface). The module processor core is active, and the 26 MHz reference clock frequency is used.

If low power mode configuration is disabled, as it is by default (see the AT commands manual [2], +UPSV AT command, for details), the module remains in active mode. Otherwise, if low power mode configuration is enabled, the module enters low power idle mode (and deep-sleep mode, if enabled) whenever possible.

When the module is registered with the network and, while active mode is maintained, the receiver is periodically activated to monitor the paging channel for paging block reception.

Detailed current consumption values can be found in the SARA-S520BM10 data sheet [1].

1.5.1.5 VCC consumption in low power idle mode

The low power mode configuration is by default disabled, but it can be enabled using the +UPSV AT command (see the AT commands manual [2]).

When low power mode is enabled, the module automatically enters the low power idle mode whenever possible, but it must periodically monitor the paging channel of the current base station (paging block reception), in accordance with the LTE system requirements, even if connected mode is not enabled by the application. When the module monitors the paging channel, it wakes up to the active mode to enable the reception of the paging block. In between, the module switches to low power mode. This is known as discontinuous reception (DRX) or extended discontinuous reception (eDRX).

When low power mode configuration is enabled and the module is registered with the network, the module automatically enters the low power idle mode, and periodically wakes up to active mode to monitor the paging channel for the paging block reception in discontinuous reception (DRX) mode.

Detailed current consumption values can be found in the SARA-S520BM10 data sheet [1].

1.5.1.6 VCC consumption in deep-sleep mode

The low power mode and the PSM / eDRX configurations are by default disabled, but they can be enabled using the +UPSV and +CPSMS / +CEDRXS AT commands (see the AT commands manual [2]).

When low power mode and PSM / eDRX are enabled, whenever possible the modules automatically enter the ultra-low power PSM / eDRX deep-sleep mode, reducing current consumption down to the lowest steady value: only the RTC runs with internal 32 kHz reference clock frequency.

Detailed current consumption values can be found in the SARA-S520BM10 data sheet [1].

1.5.2 Generic digital interfaces supply output (V_INT)

The same voltage domain internally used as supply for the cellular generic digital interfaces of the SARA-S520BM10 modules (as the cellular UART, SPI, SDIO, I2C, antenna dynamic tuner interfaces and the GPIOs) is also available on the **V_INT** output pin, as illustrated in Figure 5.

The internal regulator that generates the **V_INT** supply output is a switching (DC-DC) converter, which is directly supplied from the **VCC** main supply input of the module.

The **V_INT** voltage regulator output of SARA-S520BM10 modules is disabled (i.e. 0 V) when the module is switched off, and it can be used to monitor the operating mode of the module as follows:

- When the module is off, or in deep-sleep mode, the voltage level is low (i.e. 0 V)
- When the module is on, outside deep-sleep mode, the voltage level is high (i.e. 1.8 V)

The current capability is specified in the SARA-S520BM10 data sheet [1]. The **V_INT** voltage domain can be used in place of external discrete regulator as a reference voltage rail for external components.

The **V_INT** regulator output provides internal short circuit protection to limit the start-up current and protect the device in short circuit situations. No additional external short circuit protection is required.

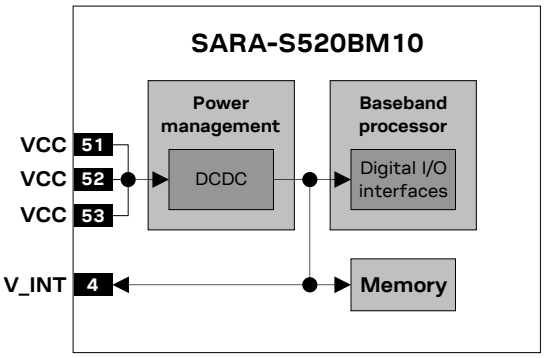

Figure 5: SARA-S520BM10 interfaces supply output (V_INT) simplified block diagram

1.5.3 GNSS backup supply input (V_BCKP_GNSS)

Backup domain (BBR and RTC) of the internal u-blox M10 GNSS chipset can be optionally supplied through the **V_BCKP_GNSS** pin, enabling the hardware backup mode when GNSS chip is switched off and allowing better TTFF, accuracy, availability, and power consumption at the next GNSS startup.

As illustrated in Figure 2, the **V_BCKP_GNSS** pin is equipped with an internal series resistor and a shunt capacitor, to limit the maximum supply ramp.

☞ To enable the GNSS RTC in hardware backup mode, a 32.768 kHz clock must also be applied (see section 1.14).

1.6 System function interfaces

1.6.1 Module power-on

1.6.1.1 Switch-on events

When the SARA-S520BM10 modules are in the not-powered mode (i.e. switched off, with the **VCC** module supply not applied), the switch-on routine can be triggered by:

- Applying a voltage at **VCC** module supply input within the operating range (see SARA-S520BM10 data sheet [1]).

When the SARA-S520BM10 modules are in the power-off mode (i.e. switched off, but with a valid voltage present at the **VCC** module supply input) or in deep-sleep mode, they can be switched on or they can be woken up as following:

- Forcing a low level at the **PWR_ON** input pin (normally high due to internal pull-up) for a valid time period (see SARA-S520BM10 data sheet [1]).

As illustrated in Figure 6, the **PWR_ON** input pin is equipped with an internal pull-up resistor. Detailed electrical characteristics with voltages and timings are described in SARA-S520BM10 data sheet [1].

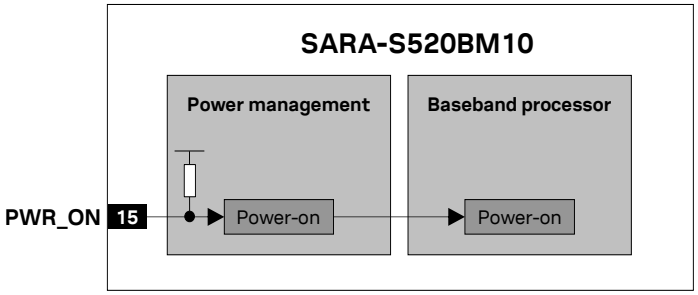

Figure 6: SARA-S520BM10 PWR_ON input equivalent circuit description

1.6.1.2 Switch-on sequence from not-powered mode

Figure 7 shows the SARA-S520BM10 switch-on sequence from not-powered mode:

- The external power supply is applied to the **VCC** module pins, representing the start-up event.
- All the generic digital pins are tri-stated until the switch-on of their supply source (**V_INT**).
- The baseband core and all digital pins are held in reset state; then, any digital pin is set in the correct sequence from the reset state to the default operational configured state. The duration of this phase differs within generic digital interfaces.
- If enabled, a greeting message is sent on the **RXD** pin (for more details, see the AT commands manual [2], +CSGT AT command).
- The module is ready to operate after all interfaces are configured.

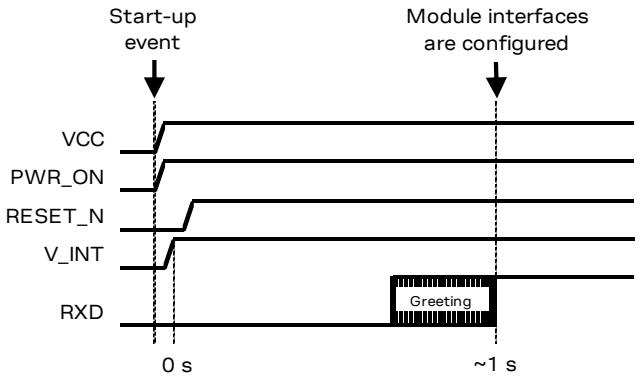

Figure 7: SARA-S520BM10 switch-on sequence description from not-powered mode

1.6.1.3 Switch-on / early wake-up sequence from power-off / deep-sleep mode

Figure 8 shows the SARA-S520BM10 modules switch-on or early wake-up sequence respectively from the power-off or deep-sleep mode:

- The external power supply is still applied to the VCC module pins, with the module being previously switched off (e.g. by the +CPWROFF AT command), or with the module being previously entered deep-sleep mode.
- The **PWR_ON** pin is held low for a valid time period, representing the start-up event.
- All the generic digital pins are tri-stated until the switch-on of their supply source (**V_INT**).
- The baseband core and all digital pins are held in reset state; then, any digital pin is set in the correct sequence from the reset state to the default operational configured state. The duration of this phase differs within generic digital interfaces.
- If enabled, a greeting message is sent on the **RXD** pin (for more details, see the AT commands manual [2], +CSGT AT command).
- The module is ready to operate after all interfaces are configured.

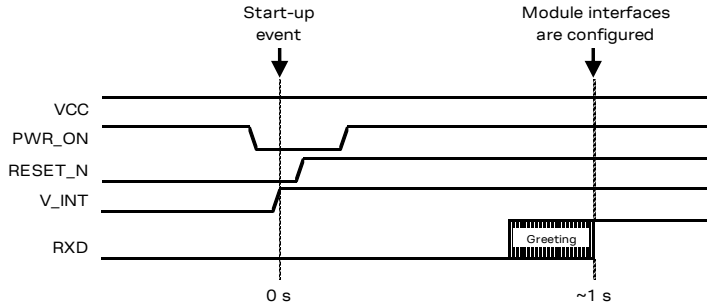

Figure 8: SARA-S520BM10 switch-on / early wake-up sequence description from power-off / deep-sleep mode

1.6.1.4 General considerations for the switch-on procedure

If the greeting text is not supported or not used by the external application to detect that the module is ready to reply to AT commands, then the only way of checking it is polling. The external application can start sending “AT” after that the **CTS** line is set to the ON state (if UART is used with HW flow control enabled, which is by default where supported), but any AT command sent before the time when the module is ready to reply may be not buffered and may be lost.

☞ It is highly recommended to monitor:
- the **V_INT** pin, to sense the start of the SARA-S520BM10 module switch-on sequence
- the **GPIO** pin configured to give module status indication or module operating mode indication (see AT commands manual [2], +UGPIOC), to sense when the module is ready to operate

☞ No voltage driven by an external application should be applied to any generic digital interface of the module (as the cellular UART, SPI, SDIO, I2C, antenna dynamic tuner interfaces and the GPIOs) before the initialization of the interfaces is finished, detectable by the “greeting text” (if enabled) or by **CTS** line going low (if HW flow control is enabled, as it is by default).

☞ The duration of the SARA-S520BM10 modules’ switch-on routine can vary depending on the application / network settings and the concurrent module activities: Figure 7 and Figure 8 only show indicative typical timings.

☞ It is highly recommended to avoid an abrupt removal of the **VCC** power supply once the boot of SARA-S520BM10 modules has been triggered.

1.6.2 Module power-off

1.6.2.1 Switch-off events

The proper graceful power-off of the SARA-S520BM10 modules, with storage of the current parameter settings in the non-volatile memory of the module and a clean network detach, can be triggered by:

- AT+CPWROFF command (see AT commands manual [2])
- Forcing a low level at the **PWR_ON** input pin (normally high due to internal pull-up) for a valid time period (see SARA-S520BM10 data sheet [1]).

☞ The methods above are recommended to properly switch off the SARA-S520BM10 modules.

A faster power-off procedure of the modules, with storage of the current parameter settings in the module's non-volatile memory, but without a clean network detach, can be triggered by:

- AT+CFUN=10 command (see AT commands manual [2])
- Forcing a rising edge at the GPIO pin configured with faster power-off function (see section 1.11, faster switch-off)

☞ The graceful switch-off procedure is preferred to the faster emergency power-off procedure. Frequent switching off without performing a clean network detach is not recommended.

An abrupt emergency hardware shutdown of the modules, without storage of the current parameter settings in the module's non-volatile memory and without clean network detach, can be triggered by:

- Forcing a low level at the **PWR_ON** input pin (normally high due to internal pull-up) for a valid time period (see SARA-S520BM10 data sheet [1]).

☞ It is recommended to avoid abrupt emergency hardware shutdowns during SARA-S520BM10 modules normal operations. An abrupt software reset, consisting in asserting the **RESET_N** input, is preferred, if considered necessary (see section 1.6.2.3).

An abrupt under-voltage shutdown occurs on SARA-S520BM10 modules when the **VCC** supply is removed. If this occurs, it is not possible to perform the storing of the current parameter settings in the module's non-volatile memory or to perform the proper network detach.

☞ It is highly recommended to avoid an abrupt removal of the **VCC** supply during SARA-S520BM10 modules normal operations. An abrupt software reset, consisting in asserting the **RESET_N** input, must be preferred, if considered necessary (see section 1.6.2.3).

☞ In case of applications where an abrupt power removal cannot be avoided, it is recommended to set the **RESET_N** input line at the low logic level as soon as the power failure in the supply source is detected, so that the under-voltage shutdown may be executed more safely since ~405 ms after the falling edge at the **RESET_N** input line.

An over-temperature or an under-temperature shutdown occurs on the SARA-S520BM10 modules when the temperature measured within the module reaches the dangerous area, if the optional "smart temperature supervisor" feature is enabled by the +USTS AT command. For more details, see SARA-S520BM10 data sheet [1] and the AT commands manual [2].

1.6.2.2 Switch-off sequence by +CPWROFF AT command

Figure 9 describes the switch-off sequence of the modules started by the +CPWROFF AT command, allowing storage of parameter settings in the non-volatile memory and a clean network detach:

- When the +CPWROFF AT command is sent the module starts the switch-off routine.
- Then the module replies OK on the AT interface: the switch-off routine is in progress.
- At the end of the switch-off routine, all the digital pins are tri-stated and all the internal voltage regulators are turned off, including the generic digital interfaces supply (**V_INT**).
- Then, the module remains in switch-off mode as long as a switch-on event does not occur (e.g. applying a low level to **PWR_ON**), or enters not-powered mode if the **VCC** supply is removed.

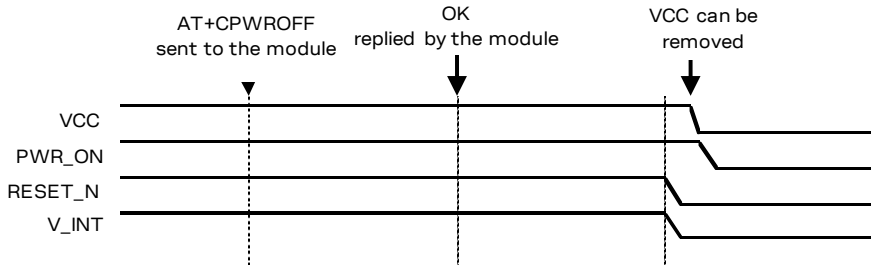

Figure 9: SARA-S520BM10 modules switch-off sequence by the +CPWROFF AT command

1.6.2.3 Switch-off sequence by toggling the PWR_ON input pin

Figure 10 describes the switch-off sequence of the modules started by toggling the **PWR_ON** input pin, allowing storage of parameter settings in the non-volatile memory and a clean network detach:

- When a low pulse with appropriate time duration is applied at the **PWR_ON** input pin, the module starts the switch-off routine.
- At the end of the switch-off routine, all the digital pins are tri-stated and all the internal voltage regulators are turned off, including the generic digital interfaces supply (**V_INT**).
- Then, the module remains in switch-off mode as long as a switch-on event does not occur (e.g. applying a low level to **PWR_ON**), or enters not-powered mode if the **VCC** supply is removed.

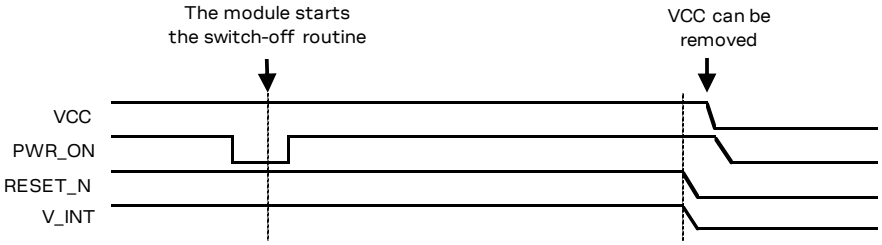

Figure 10: SARA-S520BM10 modules switch-off sequence by toggling the PWR_ON input pin

1.6.2.4 General considerations for the switch-off procedure

☞ It is highly recommended to monitor the **V_INT** pin to sense the end of the switch-off sequence.

☞ The duration of each phase in the SARA-S520BM10 modules' switch-off routines can largely vary, depending on the application / network settings and the concurrent module activities.

☞ It is highly recommended to avoid an abrupt removal of the **VCC** supply before that the **V_INT** output of the modules goes low: **VCC** supply can be removed only after **V_INT** goes low.

☞ In case of applications where an abrupt power removal cannot be avoided, it is recommended to set the **RESET_N** input line at the low logic level as soon as the power failure in the supply source is detected, so that the under-voltage shutdown may be executed more safely since ~405 ms after the falling edge at the **RESET_N** input line.

1.6.3 Module reset

SARA-S520BM10 modules can be gracefully reset (re-booted), triggering the storage of the current parameter settings in the non-volatile memory of the module and performing a clean network detach procedure, by:

- AT+CFUN=16 command (see AT commands manual [2] for further details).

An abrupt software reset of the modules, without storage of the current parameter in the module's non-volatile memory and without proper network detach, can be triggered by:

- Forcing a low level on the **RESET_N** pin (normally high due to internal pull-up) for a valid time period (see the SARA-S520BM10 data sheet [1]).

☞ If considered necessary, an abrupt software reset must be preferred to an abrupt emergency hardware shutdown or an abrupt removal of the **VCC** supply.

☞ In case of applications where an abrupt power removal cannot be avoided, it is recommended to set the **RESET_N** input line at the low logic level as soon as the power failure in the supply source is detected, so that the under-voltage shutdown may be executed more safely since ~405 ms after the falling edge at the **RESET_N** input line.

As described in Figure 11, the **RESET_N** input pin is directly connected to the processor core, with an integrated active pull-up, in order to perform an abrupt software reset when asserted, excluding the power management unit. Detailed electrical characteristics with voltages and timings are described in the SARA-S520BM10 data sheet [1].

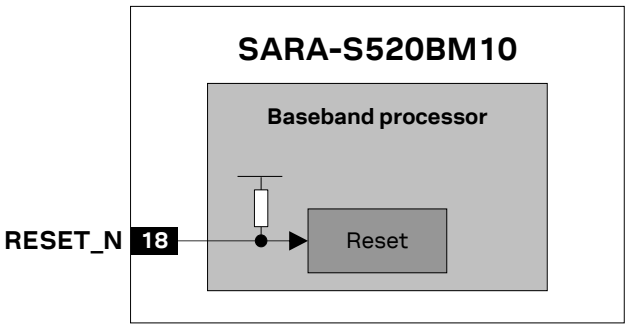

Figure 11: SARA-S520BM10 RESET_N input equivalent circuit description

1.7 Antenna interfaces

1.7.1 Cellular antenna RF interface (ANT)

SARA-S520BM10 modules provide an RF interface for connecting the external cellular antenna. The **ANT** pin represents the RF input/output for transmission and reception of LTE RF signals.

The **ANT** pin has a nominal characteristic impedance of 50 Ω and must be connected to the Tx / Rx cellular antenna through a 50 Ω transmission line to allow proper RF transmission and reception.

1.7.1.1 Cellular antenna RF interface requirements

Table 6 summarizes the requirements for the cellular antenna RF interface. See section 2.4.2 for suggestions to correctly design antennas circuits compliant with these requirements.

⚠ The antenna circuits affect the RF compliance of the device integrating SARA-S520BM10 modules with applicable required certification schemes (for more details see section 4). RF performance is optimized by fulfilling the requirements for the cellular antenna RF interface (**ANT**) summarized in Table 6.

Item	Requirements	Remarks
Impedance	50 Ω nominal characteristic impedance	The impedance of the antenna RF connection must match the 50 Ω impedance of the **ANT** port.
Frequency range	See the SARA-S520BM10 data sheet [1]	The required frequency range of the antenna connected to **ANT** port depends on the operating bands of the used cellular module and the used mobile network.
Return loss	S_{11} < -10 dB (VSWR < 2:1) recommended S_{11} < -6 dB (VSWR < 3:1) acceptable	The return loss or the S_{11}, as the VSWR, refers to the amount of reflected power, measuring how well the antenna RF connection matches the 50 Ω characteristic impedance of the **ANT** port. The impedance of the antenna termination must match as much as possible the 50 Ω nominal impedance of the **ANT** port over the operating frequency range, reducing as much as possible the amount of reflected power.
Efficiency	> -1.5 dB (> 70%) recommended > -3.0 dB (> 50%) acceptable	The radiation efficiency is the ratio of the radiated power to the power delivered to antenna input: the efficiency is a measure of how well an antenna receives or transmits. The radiation efficiency of the antenna connected to the **ANT** port needs to be enough high over the operating frequency range to comply with the Over-The-Air (OTA) radiated performance requirements, as Total Radiated Power (TRP) and the Total Isotropic Sensitivity (TIS), specified by applicable related certification schemes.
Maximum gain	According to radiation exposure limits	The power gain of an antenna is the radiation efficiency multiplied by the directivity: the gain describes how much power is radiated in the direction of peak radiation to that of an isotropic source. The maximum gain of the antenna connected to **ANT** port must not exceed the herein stated value to comply with regulatory agencies radiation exposure limits. For additional info see section 4.
Input power	> 24 dBm (> 0.25 W)	The antenna connected to the **ANT** port must support with adequate margin the maximum power transmitted by the modules.

Table 6: Summary of cellular antenna RF interface requirements

1.7.2 GNSS / Satellite antenna RF interface (ANT_GNSS_SAT)

SARA-S520BM10 modules provide an RF interface pin for connecting the external GNSS / Satellite antenna. The **ANT_GNSS_SAT** pin is the RF antenna I/O interface for GNSS RF signals reception and for Satellite RF signals transmission and reception.

The **ANT_GNSS_SAT** pin has a nominal characteristic impedance of 50 Ω and must be connected to the GNSS / Satellite antenna through a 50 Ω transmission line to allow proper RF signals transmission and reception. As shown in Figure 1, the GNSS / Satellite RF interface is designed with an internal DC block, suitable for both active and passive receiving antennas.

The reception of both Satellite and GNSS RF signals is optimized due to the internal LNA-SAW-LNA chain in front of the Satellite receiver integrated in the u-blox UBX-R52 Satellite / Cellular chipset, plus an additional SAW filter in front of the u-blox M10 GNSS receiver chipset.

1.7.2.1 GNSS / Satellite antenna RF interface requirements

As indicated in the ORBCOMM conformity section 4.5, to launch a product onto satellite networks, the product integrating the SARA-S520BM10 module requires a Type Approval certificate from ORBCOMM satellite network operator.

If the final product integrating the SARA-S520BM10 module uses one of the ORBCOMM-specified Satellite antennas, without any change in the antenna or cable, the ORBCOMM Type Approval process will be granted in a simplified process (the so-called green line process).

☞ We recommend contacting ORBCOMM to get the list of pre-certified Satellite antennas specified by ORBCOMM for the Satellite RF operations.

The use of Satellite antennas other than the ones pre-certified by ORBCOMM is possible, but in such case the full ORBCOMM Type Approval tests will be required for the final product.

Table 7 summarizes the requirements for the GNSS / Satellite antenna RF interface. See section 2.4.3 for suggestions to correctly design antennas circuits compliant with these requirements.

Item	Requirements	Remarks
Impedance	50 Ω nominal characteristic impedance	The impedance of the antenna RF connection must match the 50 Ω impedance of the **ANT_GNSS_SAT** port.
Frequency range	Satellite Rx: 1525 to 1559 MHz GNSS Rx 1559 to 1605 MHz Satellite Tx: 1626.5 to 1660.5 MHz	The required GNSS frequency range of the GNSS antenna radiating element connected to **ANT_GNSS_SAT** port depends on the selected GNSS constellations.
Return loss	S_{11} < -10 dB (VSWR < 2:1) recommended S_{11} < -6 dB (VSWR < 3:1) acceptable	The return loss or the S_{11}, as the VSWR, refers to the amount of reflected power, measuring how well the antenna RF connection matches the 50 Ω characteristic impedance of the **ANT_GNSS_SAT** port over the operating frequency range.
Gain (passive antenna)	> 4 dBic	The gain of a passive antenna is the radiation efficiency multiplied by the directivity, describing the power radiated in the direction of peak radiation to that of an isotropic source. It is important to provide good antenna visibility to the sky, using antennas with good radiation pattern in the sky direction, according to related antenna placement.
Polarization	RHCP	GNSS / Satellite signals are Right-Hand Circular Polarized.
Noise figure (GNSS / Satellite Rx active antenna)	< 2 dB recommended	Since GNSS / Satellite signals are very weak, any amount of noise degrades all the sensitivity figures of the receiver: active antennas with LNA with a low noise figure are recommended.

Table 7: Summary of GNSS / Satellite antenna RF interface requirements

1.7.3 Cellular antenna detection interface (ANT_DET)

The antenna detection is based on ADC measurement. The **ANT_DET** pin is an analog-to-digital converter (ADC) provided to sense the presence of the external cellular antenna.

The antenna detection function provided by **ANT_DET** pin is an optional feature that can be implemented if the application requires it. The antenna detection is forced by the +UANTR AT command. See the AT commands manual [2] for more details on this feature.

The **ANT_DET** pin generates a DC current (for detailed characteristics see the SARA-S520BM10 data sheet [1]) and measures the resulting DC voltage, thus determining the resistance from the antenna connector provided on the application board to GND. So, the requirements to achieve antenna detection functionality are the following:

- an RF antenna assembly with a built-in resistor (diagnostic circuit) must be used
- an antenna detection circuit must be implemented on the application board

See section 2.4.5 for antenna detection circuit on application board and diagnostic circuit on antenna assembly design-in guidelines.

1.8 SIM interface

1.8.1 SIM card interface

SARA-S520BM10 modules provide on the **VSIM**, **SIM_IO**, **SIM_CLK** and **SIM_RST** pins a high-speed SIM/ME interface including automatic detection and configuration of the voltage required by the connected SIM card or chip.

Both 1.8 V and 3 V SIM types are supported. Activation and deactivation with automatic voltage switch from 1.8 V to 3 V are implemented, according to ISO-IEC 7816-3 specifications. The **VSIM** supply output provides internal short circuit protection to limit start-up current and protects the SIM to short circuits.

1.8.2 SIM card detection interface (GPIO5)

The **GPIO5** pin can be configured as an external interrupt to detect the SIM card mechanical / physical presence. The pin can be configured as input with an internal active pull-down enabled, and it can sense SIM card presence only if cleanly connected to the mechanical switch of a SIM card holder as described in section 2.5:

- Low logic level at **GPIO5** input pin is recognized as SIM card not present
- High logic level at **GPIO5** input pin is recognized as SIM card present

The SIM card detection function provided by **GPIO5** pin is an optional feature that can be implemented or not according to the application requirements. For more details about “SIM card detection” feature, see the AT commands manual [2], +UGPIOC, +CIND and +CMER AT commands.

If the “SIM card detection” feature is enabled in the application by the dedicated +UGPIOC AT command, then it is recommended to also enable the additional “SIM card hot insertion/removal” feature by the dedicated +UDCONF=50 AT command, to enable / disable the SIM interface upon detection of the external SIM card physical insertion / removal. For more details about the “SIM card hot insertion/removal” feature, see the AT commands manual [2], +UDCONF=50 AT command.

1.9 Data communication interfaces

SARA-S520BM10 modules provide the following serial communication interfaces:

- UART interfaces, for communications with host application processor. See section 1.9.1.
- USB 2.0 compliant interface, for diagnostic only. See section 1.9.2.
- SPI interfaces, for diagnostic only. See section 1.9.3.
- SDIO interface, for diagnostic only. See section 1.9.4.
- I2C interface, for communications with external I2C devices. See section 1.9.5.

1.9.1 UART interfaces

1.9.1.1 UART features

SARA-S520BM10 modules include 1.8 V unbalanced asynchronous serial interfaces for communications with external host application processor. UART interfaces can be configured by AT commands (see the AT commands manual [2], +USIO AT command) in the following variants:

- **Variant 0** (default configuration), consisting in a single UART interface on **RXD**, **TXD**, **CTS**, **RTS**, **DTR**, **RI** pins, supporting:
  - AT commands,
  - Data communication,
  - Multiplexer protocol functionality (see 1.9.1.4),
  - FW update by FOAT,
  - FW update by the u-blox EasyFlash tool

  The following lines are provided:

  - Data lines (**RXD** as output, **TXD** as input),
  - Hardware flow control lines (**CTS** as output, **RTS** as input),
  - Modem status and control lines (**DTR** as input, **RI** as output)
- **Variant 1**, consisting in a single UART interface on **RXD**, **TXD**, **CTS**, **RTS**, **DTR**, **DSR**, **DCD**, **RI** pins, supporting:
  - AT commands,
  - Data communication,
  - Multiplexer protocol functionality (see 1.9.1.4),
  - FW update by FOAT,
  - FW update by the u-blox EasyFlash tool

  The following lines are provided:

  - Data lines (**RXD** as output, **TXD** as input),
  - Hardware flow control lines (**CTS** as output, **RTS** as input),
  - Modem status and control lines (**DTR** as input, **DSR** as output, **DCD** as output, **RI** as output)

- **Variants 2, 3 and 4**, consisting in two UART interfaces (primary UART on **RXD**, **TXD**, **CTS**, **RTS** pins, and auxiliary UART on **DCD**, **DTR**, **RI**, **DSR** pins) plus ring indicator function:
  - Primary UART interface supports:
    - AT commands,
    - Data communication,
    - Multiplexer protocol functionality (see 1.9.1.4),
    - FW update by FOAT,
    - FW update by the u-blox EasyFlash tool

    The following lines are provided:
    - Data lines (**RXD** as output, **TXD** as input),
    - Hardware flow control lines (**CTS** as output, **RTS** as input)
  - Auxiliary UART interface supports:
    - AT commands (variant 2 only),
    - Data communication (variant 2 only),
    - FW update by FOAT (variant 2 only),
    - Diagnostic trace log (variant 3 only),
    - GNSS tunneling (variant 4 only)

    The following lines are provided:
    - Data lines (**DCD** as data output, **DTR** as data input),
    - Hardware flow control lines (**RI** as flow control output, **DSR** as flow control input)
  - Ring indicator function over the GPIO pin configured for this purpose (see section 1.11)

☞ When +USIO variant 4 is set, auxiliary UART interface does not support flow control and status of its CTS line (**RI** pin) can be ignored.

UART general features, valid for all variants, are:

- Serial port with RS-232 functionality conforming to the ITU-T V.24 recommendation [4], with CMOS compatible levels (0 V for low data bit or ON state, and 1.8 V for high data bit or OFF state)
- Hardware flow control (default value) or none flow control are supported
- UART power saving indication available on the hardware flow control output, if hardware flow control is enabled: the line is driven to the OFF state when the module is not prepared to accept data by the UART interface
- One-shot autobauding is supported and it is enabled by default: automatic baud rate detection is performed only once, at module start up. After the detection, the module works at the fixed baud rate (the detected one) and the baud rate can be changed via AT command
- The default frame format is 8N1 (8 data bits, no parity, 1 stop bit)

SARA-S520BM10 modules are designed to operate as cellular modems, i.e. as the data circuit-terminating equipment (DCE) according to the ITU-T V.24 recommendation [4]. A host application processor connected to the module UART interface represents the data terminal equipment (DTE).

☞ UART signal names of the cellular modules conform to the ITU-T V.24 recommendation [4]: e.g. **TXD** line represents data transmitted by the DTE (host processor output) and received by the DCE (module input).

SARA-S520BM10 modules' UART interface is by default configured for AT commands: the module waits for AT command instructions and interprets all the characters received as commands to execute. All the functionalities supported by SARA-S520BM10 modules can be in general set and configured by AT commands:

- AT commands according to 3GPP TS 27.007 [5], 3GPP TS 27.005 [6], 3GPP TS 27.010 [7]
- u-blox AT commands (see the AT commands manual [2])

The UART interfaces settings can be suitably configured by AT commands (for more details, see the AT commands manual [2]).

Figure 12 describes the 8N1 frame format, where 8N1 means 8 data bits, no parity, 1 stop bit

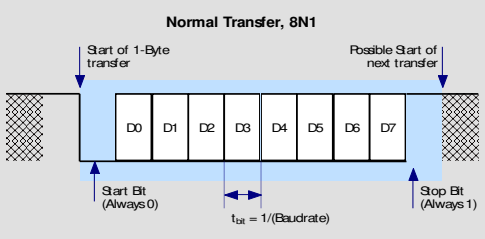

Figure 12: UART default frame format 8N1, with fixed baud rate

1.9.1.2 UART signals behavior

At the end of the module boot sequence (see Figure 7, Figure 8), the module is by default in active mode, and the UART interface is initialized and enabled as AT commands interface.

The configuration and behavior of the UART signals after the boot sequence are described below:

- The module data output lines (**RXD** only if USIO variant 0 or 1 is set; **RXD** and **DCD** if USIO variant 2, 3 or 4 is set) are set by default to the OFF state (high level) at UART initialization. The module holds these lines in the OFF state until the module transmits some data.
- The module data input lines (**TXD** only if USIO variant 0 or 1 is set; **TXD** and **DTR** if USIO variant 2, 3 or 4 is set) are assumed to be controlled by the external host once UART is initialized. The data input lines have an internal active pull-up enabled.

1.9.1.3 UART and power saving

The power saving configuration is controlled by the AT+UPSV command (for the complete description, see the AT commands manual [2]). When power saving is enabled, the module automatically enters idle mode or deep-sleep mode whenever possible, and otherwise the active mode is maintained by the module (see section 1.4 for definition and description of module operating modes referred to in this section). The AT+UPSV command configures both the module power saving and the UART behavior in relation to the power saving.

Four different power saving configurations can be set by the AT+UPSV command:

- AT+UPSV=0, power saving disabled: module forced on active mode and UART interface enabled (default)
- AT+UPSV=1, power saving enabled: UART is cyclically enabled and module enters idle mode or deep-sleep mode automatically whenever possible
- AT+UPSV=2, power saving enabled and controlled by the UART **RTS** input line (not supported if HW flow control is enabled)
- AT+UPSV=3, power saving enabled and controlled by the UART **DTR** input line (not supported if +USIO variant 2, 3 or 4 is set)
- AT+UPSV=4, power saving enabled and behavior equal to AT+UPSV=1

The different power saving configurations that can be set by the +UPSV AT command are described in detail in the following subsections. Table 8 summarizes the UART interface communication process in the different power saving configurations, in relation with HW flow control settings and **RTS** and **DTR** input lines status. For more details on the +UPSV AT command description, see the AT commands manual [2].

AT+UPSV	HW flow control	RTS line	DTR line	Communication during idle mode and wake-up
0	Enabled (AT&K3)	ON	ON or OFF	Data sent by the DTE are correctly received by the module. Data sent by the module are correctly received by the DTE.
0	Enabled (AT&K3)	OFF	ON or OFF	Data sent by the DTE are correctly received by the module. Data sent by the module is buffered by the module and will be correctly received by the DTE when it is ready to receive data (i.e. **RTS** line will be ON).
0	Disabled (AT&K0)	ON or OFF	ON or OFF	Data sent by the DTE are correctly received by the module. Data sent by the module are correctly received by the DTE if it is ready to receive data, otherwise data are lost.
1 or 4	Enabled (AT&K3)	ON	ON or OFF	Data sent by the DTE should be buffered by the DTE and will be correctly received by the module when active mode is entered. Data sent by the module are correctly received by the DTE.
1 or 4	Enabled (AT&K3)	OFF	ON or OFF	Data sent by the DTE should be buffered by the DTE and will be correctly received by the module when active mode is entered. Data sent by the module are buffered by the module and will be correctly received by the DTE when it is ready to receive data (i.e. **RTS** line will be ON).
1 or 4	Disabled (AT&K0)	ON or OFF	ON or OFF	The first character sent by the DTE is lost, but after ~15 ms the UART and the module are waked up: recognition of subsequent characters occurs after the complete UART / module wake-up. Data sent by the module are correctly received by the DTE if it is ready to receive data, otherwise data are lost.
2	Enabled (AT&K3)	ON or OFF	ON or OFF	Not applicable: HW flow control cannot be enabled with AT+UPSV=2.
2	Disabled (AT&K0)	ON	ON or OFF	Data sent by the DTE are correctly received by the module. Data sent by the module are correctly received by the DTE if it is ready to receive data, otherwise data are lost.
2	Disabled (AT&K0)	OFF	ON or OFF	Data sent by the DTE are lost. Data sent by the module are correctly received by the DTE if it is ready to receive data, otherwise data are lost.
3	Enabled (AT&K3)	ON	ON	Data sent by the DTE are correctly received by the module. Data sent by the module are correctly received by the DTE.
3	Enabled (AT&K3)	ON	OFF	Data sent by the DTE are lost. Data sent by the module are correctly received by the DTE.
3	Enabled (AT&K3)	OFF	ON	Data sent by the DTE are correctly received by the module. Data sent by the module are buffered by the module and will be correctly received by the DTE when it is ready to receive data (i.e. **RTS** line will be ON).
3	Enabled (AT&K3)	OFF	OFF	Data sent by the DTE are lost. Data sent by the module are buffered by the module and will be correctly received by the DTE when it is ready to receive data (i.e. **RTS** line will be ON).
3	Disabled (AT&K0)	ON or OFF	ON	Data sent by the DTE are correctly received by the module. Data sent by the module are correctly received by the DTE if it is ready to receive data, otherwise data are lost.
3	Disabled (AT&K0)	ON or OFF	OFF	Data sent by the DTE are lost. Data sent by the module are correctly received by the DTE if it is ready to receive data, otherwise data are lost.

Table 8: UART and power-saving summary

AT+UPSV=0: power saving disabled, fixed active mode

The module does not enter idle mode and the UART interface is enabled (data can be sent and received): the **CTS** line is always held in the ON state after UART initialization. This is the default configuration.

AT+UPSV=1 or AT+UPSV=4: power saving enabled

When the AT+UPSV=1 command is issued by the DTE, the UART is disabled after the timeout set by the second parameter of the +UPSV AT command (for more details, see the AT commands manual [2]).

Afterwards, the UART is periodically enabled to receive or send data and, if data has not been received or sent over the UART, the interface is automatically disabled whenever possible according to the timeout configured by the second parameter of the +UPSV AT command.

The module automatically enters the idle mode whenever possible, but it wakes up to active mode according to the UART periodic wake-up so that the module cyclically enters the idle mode and the active mode. Additionally, the module wakes up to active mode according to any required activity related to the network or any other required activity related to the functions / interfaces of the module.

The module automatically enters the deep-sleep mode, according to the PSM / eDRX settings, and according to the concurrent activities executed by the module (e.g. GNSS activities); when the module is in deep-sleep mode, UART is not functional.

The UART is enabled, and the module does not enter idle mode, in the following cases:

- During the periodic UART wake-up to receive or send data
- If the module needs to transmit some data over the UART (e.g. URC)
- During a PSD data call with external context activation
- If a character is sent by the DTE with HW flow control disabled, the first character sent causes the system wake-up due to the “wake-up via data reception” feature described in a following subsection, and the UART will be then kept enabled after the last data received according to the timeout set by the second parameter of the AT+UPSV=1 command

The module, when not in deep-sleep mode, periodically wakes up from idle mode to active mode to monitor the paging channel of the current base station (paging block reception), according to DRX and eDRX specifications, and according to +CEDRXS / +CEDRXRDP AT commands setting. The time period between two paging receptions is defined by the current base station (i.e. by the network); the eDRX parameters can be set by the module but are then negotiated with the current base station (i.e. by the network).

When the module is not registered with a network, the UART is enabled for ~30 ms, and then, if data has not been received or sent, the UART is disabled for ~31 s, and afterwards the interface is enabled again.

The module active mode duration depends on:

- Network parameters, related to the time interval for the paging block reception
- Duration of UART enable time in absence of data reception (~30 ms)
- The time period from the last data received at the serial port during the active mode: the module does not enter idle mode until a timeout expires. The second parameter of the +UPSV AT command configures this timeout (see the AT commands manual [2]).
  The active mode duration can be extended indefinitely since every subsequent character, received during the active mode, resets and restarts the timer.

The hardware flow control output (**CTS** line) indicates when the UART interface is enabled (data can be sent and received over the UART), if HW flow control is enabled, as illustrated in Figure 13: UART interface of the module is enabled when CTS is ON or low level; and disabled if CTS is OFF or high level.

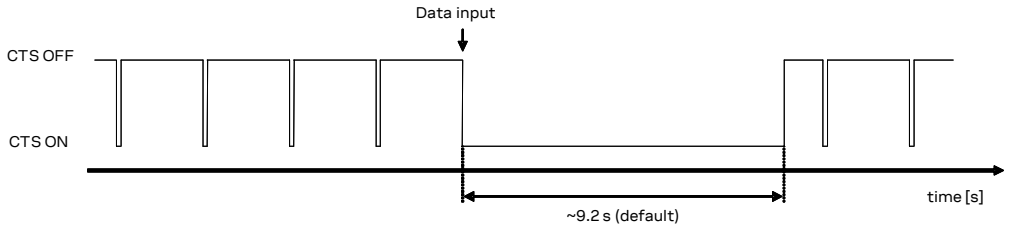

Figure 13: CTS behavior with power saving enabled (AT+UPSV=1) and HW flow control enabled:

AT+UPSV=2: power saving enabled and controlled by the RTS line

☞ This configuration can only be enabled with the module hardware flow control disabled by AT&K0 command.

The UART interface is immediately disabled after the DTE sets the **RTS** line to OFF.

Then, the module automatically enters idle mode whenever possible according to any required activity related to the network or any other required activity related to the functions / interfaces of the module.

The module automatically enters the deep-sleep mode, according to the PSM / eDRX settings, and according to the concurrent activities executed by the module (e.g. GNSS activities); when the module is in deep-sleep mode, UART is not functional.

The UART is disabled as long as the **RTS** line is held to OFF, but the UART is enabled in the following cases:

- If the module needs to transmit some data over the UART (e.g. URC)
- During a PSD data call with external context activation

When an OFF-to-ON transition occurs on the **RTS** input line, the UART is re-enabled and the module, if it was in idle mode, switches from idle to active mode after ~15 ms: this is the UART and module "wake-up time".

If the **RTS** line is set to ON by the DTE, then the module is not allowed to enter the idle mode or deep-sleep mode and the UART is kept enabled until the **RTS** line is set to OFF.

AT+UPSV=3: power saving enabled and controlled by the DTR line

☞ This configuration can only be enabled with the +USIO variant set to 0 or 1 (single UART interface).

The UART interface is immediately disabled after the DTE sets the **DTR** line to OFF.

Then, the module automatically enters idle mode whenever possible according to any required activity related to the network or any other required activity related to the functions / interfaces of the module.

The module automatically enters the deep-sleep mode, according to the PSM / eDRX settings, and according to the concurrent activities executed by the module (e.g. GNSS activities); when the module is in deep-sleep mode, UART is not functional.

The UART is disabled as long as the **DTR** line is held to OFF, but the UART is enabled in case the module needs to transmit some data over the UART (e.g. URC).

When an OFF-to-ON transition occurs on the **DTR** input line, the UART is re-enabled and the module, if it was in idle mode, switches from idle to active mode after ~15 ms: this is the UART and module "wake-up time".

If the **DTR** line is set to ON by the DTE, then the module is not allowed to enter the idle mode or deep-sleep mode and the UART is kept enabled until the **DTR** line is set to OFF.

When the AT+UPSV=3 configuration is enabled, the **DTR** input line can still be used by the DTE to control the module behavior according to AT&D command configuration (see the AT commands manual [2]).

☞ The **CTS** output line indicates the UART power saving state as illustrated in Figure 13, if HW flow control is enabled with AT+UPSV=3.

Wake-up via data reception

The UART wake-up via data reception consists of a special configuration during idle mode of the module **TXD** input line that causes the system wake-up when an OFF-to-ON transition occurs on the **TXD** input line. In particular, the UART is enabled and the module switches from the idle mode to active mode within ~15 ms from the first character received: this is the system "wake-up time".

As a consequence, the first character sent by the DTE when the UART is disabled (i.e. the wake-up character) is not a valid communication character even if the wake-up via data reception configuration is active, because it cannot be recognized, and the recognition of the subsequent characters occurs only after the complete system wake-up (i.e. after ~15 ms).

The UART wake-up via data reception configuration is active in the following case:

- AT+UPSV=1 or AT+UPSV=4 is set

The UART wake-up via data reception configuration is not active on the **TXD** input, and therefore all the data sent by the DTE is lost, in the following cases:

- AT+UPSV=2 is set and the **RTS** line is set OFF
- AT+UPSV=3 is set and the **DTR** line is set OFF

Figure 14 and Figure 15 show examples of common scenarios and timing constraints:

- AT+UPSV=1 power saving configuration is active and the timeout from last data received to idle mode start is set to 2000 GSM frames (AT+UPSV=1,2000)
- Hardware flow control is disabled

Figure 14 shows the case where the module UART is disabled and only a wake-up is forced. In this scenario the only character sent by the DTE is the wake-up character; as a consequence, the DCE module UART is disabled when the timeout from last data received expires (2000 GSM frames without data reception, as the default case).

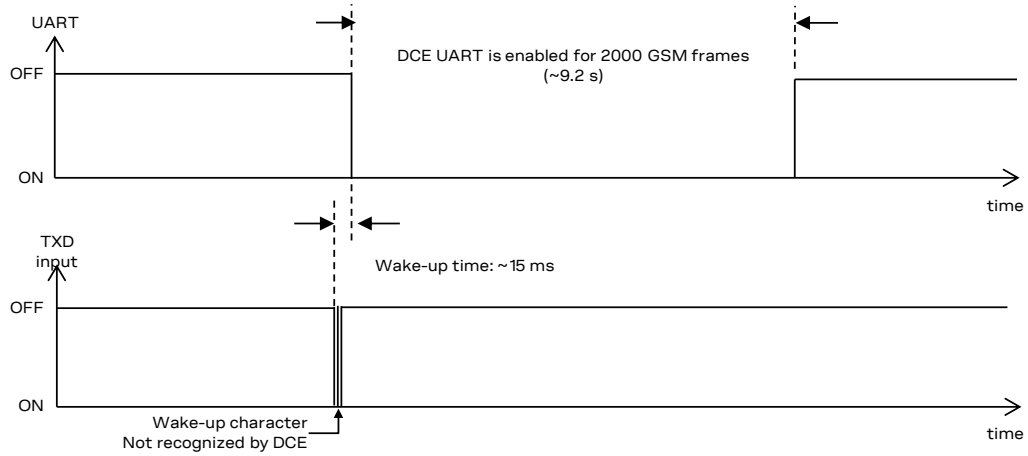

Figure 14: Wake-up via data reception without further communication

Figure 15 shows the case where in addition to the wake-up character further valid characters are sent. The wake-up character wakes up the module UART. The other characters must be sent after the "wake-up time" of ~15 ms. If this condition is satisfied, the module (DCE) recognizes characters. The module will disable the UART after 2000 GSM frames from the latest data reception.

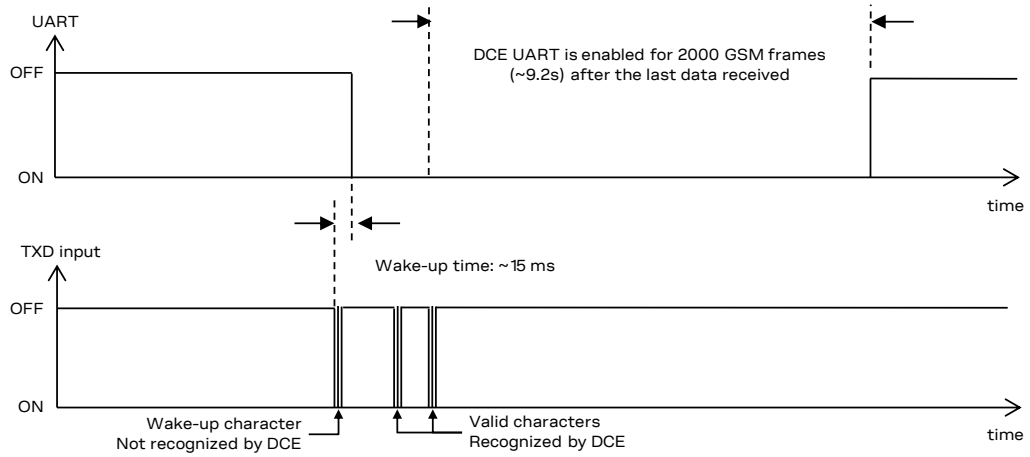

Figure 15: Wake-up via data reception with further communication

☞ The "wake-up via data reception" feature cannot be disabled.

1.9.1.4 UART multiplexer protocol

SARA-S520BM10 modules include multiplexer functionality as per 3GPP TS 27.010 [7], on the UART physical link. This is a data link protocol which uses HDLC-like framing and operates between the module (DCE) and the application processor (DTE) and allows a number of simultaneous sessions over the used physical link (UART).

When USIO variant 0 or 1 is set, the following virtual channels are defined:

- Channel 0: control channel
- Channel 1 – 3: AT commands / data communication
- Channel 4: GNSS tunneling

When USIO variant 2 is set, AT commands and data communication are available on auxiliary UART, and the following virtual channels are defined on primary UART:

- Channel 0: control channel
- Channel 1 – 2: AT commands / data communication
- Channel 3: GNSS tunneling

When USIO variant 3 is set, diagnostic trace log is available on auxiliary UART, and the following virtual channels are defined on primary UART:

- Channel 0: control channel
- Channel 1 – 3: AT commands / data communication
- Channel 4: GNSS tunneling

When USIO variant 4 is set, GNSS tunneling is available on auxiliary UART, and the following virtual channels are defined on primary UART:

- Channel 0: control channel
- Channel 1 – 3: AT commands / data communication

For more details, see the mux implementation application note [8].

1.9.2 USB interface

SARA-S520BM10 modules include a high-speed USB 2.0 compliant interface with a maximum 480 Mbit/s data rate according to the Universal Serial Bus Revision 2.0 specification [3]. The module itself acts as a USB device and can be connected to any USB host equipped with compatible drivers.

The USB interface is available for diagnostic purposes only.

The **USB_D+** / **USB_D-** lines carry the USB data / signaling, while the **VUSB_DET** input pin represents the input to enable the USB interface by applying an external valid USB VBUS voltage (5 V typical).

1.9.3 SPI interface

☞ The SPI interface is not supported by current SARA-S520BM10, except for diagnostic purposes.

SARA-S520BM10 modules include 1.8 V Serial Peripheral Interfaces available for communications with external SPI devices, or for diagnostic purposes with the module acting as SPI host.

1.9.4 SDIO interface

☞ The SDIO interface is not supported by current SARA-S520BM10, except for diagnostic purposes.

SARA-S520BM10 modules include a 1.8 V 4-bit Secure Digital Input Output interface over **SDIO_D0**, **SDIO_D1**, **SDIO_D2**, **SDIO_D3**, **SDIO_CLK** and **SDIO_CMD** pins, with the module acting as an SDIO host, available for diagnostic purposes.

1.9.5 I2C interface

SARA-S520BM10 modules include a 1.8 V I2C-bus compatible interface over the **SDA** and **SCL** pins, available to communicate with external I2C devices: the SARA-S520BM10 module acts as an I2C host that can communicate with I2C devices in accordance with the I2C bus specifications [9].

The same 1.8 V I2C-bus compatible interface is internally connected to the u-blox M10 GNSS chipset integrated in SARA-S520BM10 modules, as illustrated in Figure 2.

1.10 ADC

SARA-S520BM10 modules include an analog-to-digital converter input pin, **ADC**, configurable via a dedicated AT command (for further details, see the AT commands manual [2]).

1.11 General purpose input / output (GPIO)

SARA-S520BM10 modules include pins which can be configured as general purpose input/output or to provide custom functions via u-blox AT commands (for more details see AT commands manual [2], +UGPIOC, +UGPIOR, +UGPIOW, or related AT commands), as summarized in Table 9.

Function	Description	Default GPIO	Configurable GPIOs
General purpose output	Output to set the high or the low digital level	-	GPIO1, GPIO2, GPIO3, GPIO4, GPIO5, GPIO6, GPIO7
General purpose input	Input to sense high or low digital level	-	GPIO1, GPIO2, GPIO3, GPIO4, GPIO5, GPIO6, GPIO7
Network status indication	Output indicating cellular network status: registered, data transmission, no service	-	GPIO1, GPIO2, GPIO3, GPIO4, GPIO5, GPIO6,
SIM card detection	Input for SIM card physical presence detection, to optionally enable / disable SIM interface upon detection of external SIM card physical insertion / removal	-	GPIO5
Module status indication	Output indicating module status: power-off or deep-sleep mode versus idle, active or connected mode	-	GPIO1, GPIO2, GPIO3, GPIO4, GPIO5, GPIO6
Module operating mode indication	Output indicating module operating mode: power-off, deep-sleep or idle mode versus active or connected mode	-	GPIO1, GPIO2, GPIO3, GPIO4, GPIO5, GPIO6
Ring indicator	Output providing events indicator	-	GPIO1, GPIO2, GPIO3, GPIO4, GPIO5, GPIO6
Last gasp	Input to trigger last gasp notification	-	GPIO1, GPIO2, GPIO4, GPIO6
Time pulse output	Output providing accurate time reference, as a sequence with configurable PPS or as single time pulse, based on the GNSS system or the LTE system (CellTime™)	-	GPIO6
Faster power-off	Input with internal pull-down to trigger a faster shutdown (as AT+CFUN=10) by applying a rising edge	-	GPIO1, GPIO2, GPIO4, GPIO6
Satellite / GNSS Rx indication	Output indicating Satellite RF receiving and/or GNSS RF receiving operation in progress, to optionally control external LNA(s) and/or active antenna(s): • High with Satellite Rx, or GNSS Rx in progress, • Low otherwise	-	GPIO2
Satellite / GNSS Tx/Rx indication	Output indicating Satellite RF transmitting / receiving and/or GNSS RF receiving operation in progress: • High with Satellite Tx, Satellite Rx, or GNSS Rx in progress, • Low otherwise	-	GPIO7
Pin disabled	Tri-state with an internal active pull-down enabled	GPIO1, GPIO2, GPIO3, GPIO4, GPIO5, GPIO6, GPIO7	GPIO1, GPIO2, GPIO3, GPIO4, GPIO5, GPIO6, GPIO7

Table 9: SARA-S520BM10 modules GPIO custom functions configuration

1.12 Cellular antenna dynamic tuner interface

SARA-S520BM10 modules include two output pins, **RFCTRL1** and **RFCTRL2**, that can optionally be used to control in real time an external antenna tuning IC, as the two pins change their output value dynamically according to the specific current LTE band in use by the module. Table 10 illustrates the default factory-programmed configuration, which can be changed by dedicated AT command.

RFCTRL1	RFCTRL2	LTE frequency band in use
0	0	B71 (< 700 MHz)
0	1	B12, B13, B28, B85 (700..800 MHz)
1	0	B5, B8, B18, B19, B20, B26 (800..900 MHz)
1	1	B1, B2, B3, B4, B25, B66 (> 1000 MHz)

Table 10: SARA-S520BM10 modules antenna dynamic tuning truth table (default factory-programmed configuration)

1.13 GNSS peripheral outputs

SARA-S520BM10 modules provide the following 1.8 V peripheral output pins directly connected to the internal u-blox M10 GNSS chipset (as illustrated in Figure 2):

- The **TXD_GNSS** pin provides the UART data output of the internal u-blox GNSS chipset.

1.14 GNSS real-time clock

The internal u-blox M10 GNSS receiver contains circuitry to optionally support a real-time clock (RTC). The RTC section is in the backup power domain and can keep time while the receiver is switched off. When the receiver is switched on, it attempts to use the RTC to initialize receiver local time and, in most cases, this leads to considerably faster and more accurate first fixes.

As illustrated in Figure 2, the 32.768 kHz clock can be applied externally through the **RTC_GNSS** pin; alternatively, it can be enabled with a dedicated AT command and internally generated as long as the module does not enter deep-sleep mode or does not switch-off.

☞ To enable the GNSS RTC in hardware backup mode, the GNSS backup power domain must also be supplied (see section 1.5.3).

2 Design-in

2.1 Overview

For an optimal integration of the SARA-S520BM10 modules in the final application board, follow the design guidelines stated in this section.

Every application circuit must be suitably designed to ensure the correct functionality of the relative interface, but several points require greater attention during the design of the application device.

The following list provides a rank of importance in the application design, starting from the highest relevance:

1. Module antennas connection: **ANT** and **ANT_GNSS_SAT** pins.
   Antenna circuit directly affects the RF compliance of the device integrating a SARA-S520BM10 module with applicable certification schemes. Follow the suggestions provided in the relative section 2.4 for schematic and layout design.

2. Module supply: **VCC** and **GND** pins.
   The supply circuit affects the RF compliance of the device integrating a SARA-S520BM10 module with the applicable required certification schemes as well as the antenna circuits design. Very carefully follow the suggestions provided in the relative section 2.2.1 for schematic and layout design.

3. SIM interface: **VSIM**, **SIM_CLK**, **SIM_IO**, **SIM_RST** pins.
   Accurate design is required to ensure SIM card functionality reducing the risk of RF coupling. Carefully follow the suggestions provided in relative section 2.5 for schematic and layout design.

4. System functions: **PWR_ON** and **RESET_N** pins.
   Accurate design is required to ensure that the voltage level is well defined during operation. Carefully follow the suggestions provided in relative section 2.3 for schematic and layout design.

5. Other digital interfaces: UART, USB, SPI, SDIO, I2C, ADC, GPIOs and GNSS PIOs.
   Accurate design is required to ensure correct functionality and reduce the risk of digital data frequency harmonics coupling. Follow the suggestions provided in sections 2.6, 2.7, 2.8 and 2.9 for schematic and layout design.

6. Other supplies: **V_INT** generic digital interfaces supply.
   Accurate design is required to ensure correct functionality. Follow the suggestions provided in the corresponding section 2.2.2 for schematic and layout design.

7. GNSS backup supply and real-time clock: **V_BCKP_GNSS** and **RTC_GNSS** pins.
   Accurate design is required to ensure correct functionality. Follow the suggestions provided in sections 2.2.3 and 2.10 for schematic and layout design.

☞ It is recommended to follow the specific design guidelines provided by each manufacturer of any external part selected for the application board integrating the u-blox cellular modules.

2.2 Supply interfaces

2.2.1 Module supply (VCC)

2.2.1.1 General guidelines for VCC supply circuit selection and design

All the available **VCC** pins must be connected to the external supply minimizing the power loss due to series resistance.

GND pins are internally connected. Application design shall connect all the available pads to solid ground on the application board, since a good (low impedance) connection to external ground can minimize power loss and improve RF and thermal performance.

SARA-S520BM10 modules must be sourced through the **VCC** pins with a suitable DC power supply that should comply with the module **VCC** requirements summarized in Table 5.

The appropriate DC power supply can be selected according to the application requirements (see Figure 16) between the different possible supply sources types, which most common ones are the following:

- Switching regulator
- Low Drop-Out (LDO) linear regulator
- Rechargeable Lithium-ion (Li-Ion) or Lithium-ion polymer (Li-Pol) battery
- Primary (disposable) battery

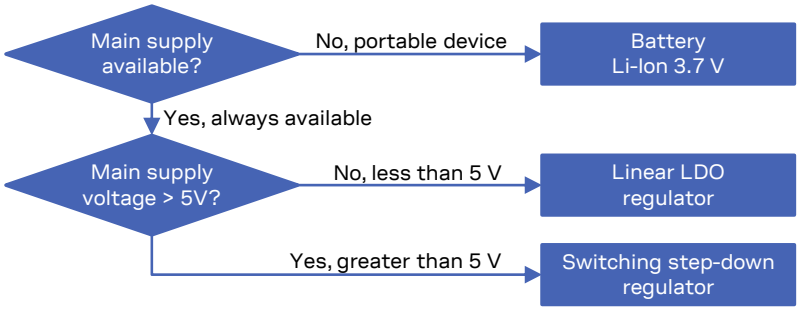

Figure 16: VCC supply concept selection

The switching step-down regulator is the typical choice when primary supply source has a nominal voltage much higher (e.g. greater than 5 V) than the operating supply voltage of SARA-S520BM10. The use of switching step-down provides the best power efficiency for the overall application and minimizes current drawn from the main supply source. See section 2.2.1.2 for design-in.

The use of an LDO linear regulator becomes convenient for a primary supply with a relatively low voltage (e.g. less or equal than 5 V). In this case, the typical 90% efficiency of the switching regulator diminishes the benefit of voltage step-down and no true advantage is gained in input current savings. On the opposite side, linear regulators are not recommended for high voltage step-down as they dissipate a considerable amount of energy in thermal power. See section 2.2.1.3 for design-in.

If SARA-S520BM10 modules are deployed in a mobile unit where no permanent primary supply source is available, then a battery will be required to provide **VCC**. A standard 3-cell Li-Ion or Li-Pol battery pack directly connected to **VCC** is the usual choice for battery-powered devices. During charging, batteries with Ni-MH chemistry typically reach a maximum voltage that is above the maximum rating for **VCC**, and should therefore be avoided. See sections 2.2.1.4, 2.2.1.5, 2.2.1.6 and 2.2.1.7 for specific design-in.

Keep in mind that the use of rechargeable batteries requires the implementation of a suitable charger circuit, which is not included in the modules. The charger circuit needs to be designed to prevent over-voltage on **VCC** pins, and it should be selected according to the application requirements. A DC-DC switching charger is the typical choice when the charging source has a high nominal voltage (e.g. ~12 V), whereas a linear charger is the typical choice when the charging source has a relatively low nominal voltage (~5 V). If both a permanent primary supply / charging source (e.g. ~12 V) and a rechargeable back-up battery (e.g. 3.7 V Li-Pol) are available at the same time as possible supply source, then a suitable charger / regulator with integrated power path management function can be selected to supply the module while simultaneously and independently charging the battery. See sections 2.2.1.6 and 2.2.1.7 for specific design-in.

An appropriate primary (not rechargeable) battery can be selected considering the maximum current specified in the SARA-S520BM10 data sheet [1] during Satellite connected mode, considering that primary cells might have weak power capability. See section 2.2.1.5 for specific design-in.

The usage of more than one DC supply at the same time should be carefully evaluated: depending on the supply source characteristics, different DC supply systems can result as mutually exclusive.

The selected regulator or battery must be able to support with adequate margin (e.g. at least twice) the highest averaged current consumption value specified in the SARA-S520BM10 data sheet [1].

The following sections highlight some design aspects for each of the supplies listed above providing application circuit design-in compliant with the module **VCC** requirements summarized in Table 5.

2.2.1.2 Guidelines for VCC supply circuit design using a switching regulator

The use of a switching regulator is suggested when the difference from the available supply rail source to the **VCC** value is high, since switching regulators provide good efficiency transforming a 12 V or greater voltage supply to the typical 3.8 V value of the **VCC** supply.

The characteristics of the switching regulator connected to **VCC** pins should meet the following prerequisites to comply with the module **VCC** requirements summarized in Table 5:

- **Power capability**: the switching regulator with its output circuit must be capable of providing a voltage value to the **VCC** pins within the specified operating range and must be capable of delivering to **VCC** pins the maximum current consumption occurring during transmissions to the Satellite system, as specified in the SARA-S520BM10 data sheet [1].
- **Low output ripple**: the switching regulator together with its output circuit must be capable of providing a clean (low noise) **VCC** voltage profile.
- **PWM mode operation**: it is preferable to select regulators with Pulse Width Modulation (PWM) mode. While in connected mode, the Pulse Frequency Modulation (PFM) mode and PFM/PWM modes transitions must be avoided to reduce noise on **VCC** voltage profile. Switching regulators can be used that are able to switch between low ripple PWM mode and high ripple PFM mode, provided that the mode transition occurs when the module changes status from the active mode to connected mode. It is permissible to use a regulator that switches from the PWM mode to the burst or PFM mode at an appropriate current threshold.

Figure 17 and the components listed in Table 11 show an example of a power supply circuit for the SARA-S520BM10 modules. In this example, the module **VCC** is supplied by a step-down switching regulator capable of delivering the maximum peak / pulse current specified for the Satellite use-case, with low output ripple and with fixed switching frequency in PWM mode operation greater than 1 MHz.

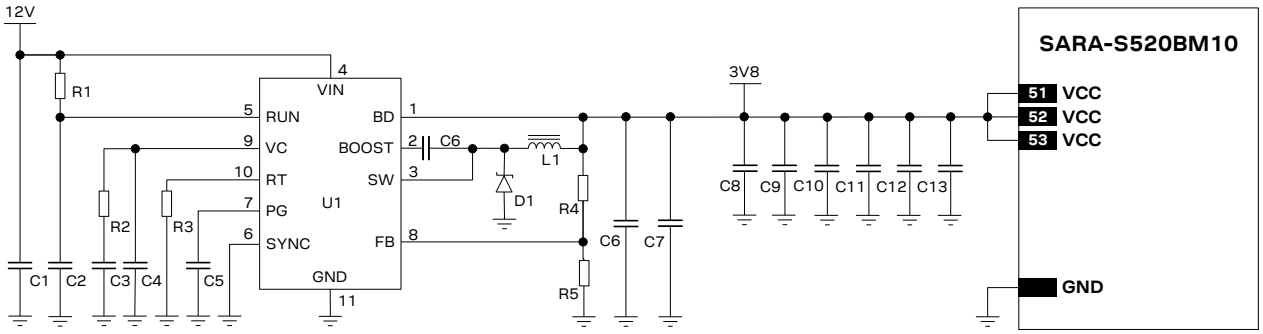

Figure 17: Example of VCC supply circuit for SARA-S520BM10 modules, using a step-down regulator

Reference	Description	Part number – manufacturer
C1	10 µF Capacitor Ceramic X7R 5750 15% 50 V	C5750X7R1H106MB – TDK
C2	10 nF Capacitor Ceramic X7R 0402 10% 16 V	GRM155R71C103KA01 – Murata
C3	680 pF Capacitor Ceramic X7R 0402 10% 16 V	GRM155R71H681KA01 – Murata
C4	22 pF Capacitor Ceramic C0G 0402 5% 25 V	GRM1555C1H220JZ01 – Murata
C5	10 nF Capacitor Ceramic X7R 0402 10% 16 V	GRM155R71C103KA01 – Murata
C6	22 µF capacitor ceramic X5R 25 V	Generic manufacturer
C7	22 µF capacitor ceramic X5R 25 V	Generic manufacturer
C8	100 nF capacitor ceramic X7R 16 V	GCM155R71C104KA55 – Murata
C9	10 nF capacitor ceramic X7R 16 V	GRT155R71C103KE01 – Murata
C10	82 pF capacitor Ceramic C0G 0402 5% 50 V	GRM1555C1H820JA01 – Murata
C11	27 pF capacitor ceramic C0G 0402 5% 50 V	GRM1555C1H270JA01 – Murata
C12	15 pF capacitor ceramic C0G 0402 5% 50 V	GJM1555C1H150JB01 – Murata
C13	330 µF capacitor Tantalum D_SIZE 6.3 V 45 mΩ	T520D337M006ATE045 - KEMET
D1	Schottky Diode 40 V 3 A	MBRA340T3G – ON Semiconductor
L1	10 µH Inductor 744066100 30% 3.6 A	744066100 – Wurth Electronics
R1	470 kΩ Resistor 0402 5% 0.1 W	Various manufacturers
R2	15 kΩ Resistor 0402 5% 0.1 W	Various manufacturers
R3	22 kΩ Resistor 0402 5% 0.1 W	Various manufacturers
R4	390 kΩ Resistor 0402 1% 0.063 W	Various manufacturers
R5	100 kΩ Resistor 0402 5% 0.1 W	Various manufacturers
U1	Step-Down Regulator MSOP10 3.5 A 2.4 MHz	LT3972IMSE#PBF – Linear Technology

Table 11: Components for the VCC supply circuit for SARA-S520BM10 modules, using a step-down regulator

See the section 2.2.1.8, and in particular Figure 22 / Table 15, for the parts recommended to be provided if the application device integrates an internal antenna.

2.2.1.3 Guidelines for VCC supply circuit design using linear regulator

The use of a linear regulator is suggested when the difference from the available supply rail source and the **VCC** value is low: linear regulators provide high efficiency when transforming a 5 V supply to a voltage value within the module **VCC** normal operating range.

The characteristics of the Low Drop-Out (LDO) linear regulator connected to **VCC** pins should meet the following prerequisites to comply with the module **VCC** requirements summarized in Table 5:

- **Power capabilities**: the LDO linear regulator with its output circuit must be capable of providing a voltage value to the **VCC** pins within the specified operating range and must be capable of delivering to **VCC** pins the maximum current consumption occurring during a transmission to the Satellite system, as specified in the SARA-S520BM10 data sheet [1].
- **Power dissipation**: the power handling capability of the LDO linear regulator must be checked to limit its junction temperature to the rated range (i.e. check the voltage drop from the maximum input voltage to the minimum output voltage to evaluate the power dissipation of the regulator).

Figure 18 and the components listed in Table 12 show an example of a power supply circuit for the SARA-S520BM10 modules, where the module **VCC** is supplied by an LDO linear regulator capable of delivering adequate maximum peak / pulse current, with suitable power handling capability.

To reduce the LDO power dissipation, it is recommended to configure the LDO linear regulator to generate a voltage supply value slightly below the maximum limit of the module **VCC** normal operating range (e.g. ~4.1 V for the **VCC**, as in the circuits described in Figure 18 and Table 12). This reduces the power on the linear regulator and improves the thermal design of the circuit.

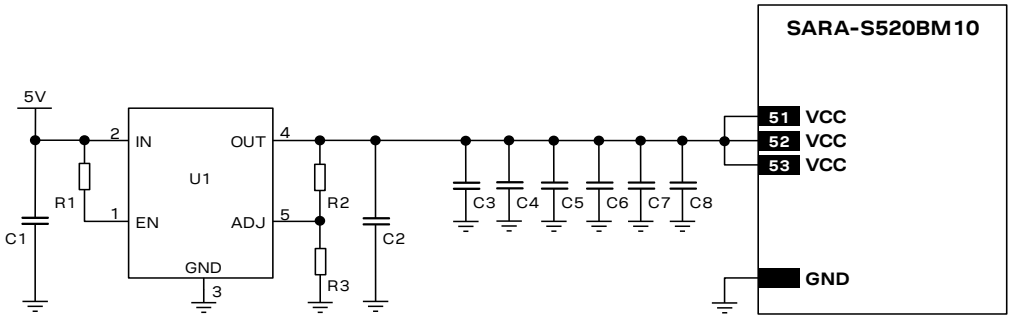

Figure 18: Example of VCC supply circuit for SARA-S520BM10 modules, using an LDO linear regulator

Reference	Description	Part number – Manufacturer
C1	1 µF capacitor ceramic X5R 6.3 V	Generic manufacturer
C2	22 µF capacitor ceramic X5R 25 V	Generic manufacturer
C3	100 nF capacitor ceramic X7R 16 V	GCM155R71C104KA55 – Murata
C4	10 nF capacitor ceramic X7R 16 V	GRT155R71C103KE01 – Murata
C5	82 pF capacitor Ceramic C0G 0402 5% 50 V	GRM1555C1H820JA01 – Murata
C6	27 pF capacitor ceramic C0G 0402 5% 50 V	GRM1555C1H270JA01 – Murata
C7	15 pF capacitor ceramic C0G 0402 5% 50 V	GJM1555C1H150JB01 – Murata
C8	330 µF capacitor Tantalum D_SIZE 6.3 V 45 mΩ	T520D337M006ATE045 - KEMET
R1	10 kΩ resistor 0.1 W	Generic manufacturer
R2	36 kΩ resistor 0.1 W	Generic manufacturer
R3	6.2 kΩ resistor 0.1 W	Generic manufacturer
U1	LDO linear regulator 3.0 A	LP38501-ADJ – Texas Instruments

Table 12: Components for VCC supply circuit for SARA-S520BM10 modules, using an LDO linear regulator

☞ See the section 2.2.1.8, and in particular Figure 22 / Table 15, for the parts recommended to be provided if the application device integrates an internal antenna.

2.2.1.4 Guidelines for VCC supply circuit design using a rechargeable battery

Rechargeable Li-Ion or Li-Pol batteries connected to the **VCC** pins should meet the following prerequisites to comply with the module **VCC** requirements summarized in Table 5:

- **Maximum pulse and DC discharge current**: the rechargeable Li-Ion battery with its related output circuit connected to the **VCC** pins must be capable of delivering the maximum current occurring during transmissions to the Satellite system, as specified in the SARA-S520BM10 data sheet [1]. The maximum discharge current is not always reported in the data sheets of batteries, but the maximum DC discharge current is typically almost equal to the battery capacity in Amp-hours divided by 1 hour.
- **DC series resistance**: the rechargeable Li-Ion battery with its output circuit must be capable of avoiding a VCC voltage drop below the operating range summarized in Table 5 during transmission.

2.2.1.5 Guidelines for VCC supply circuit design using a primary battery

The characteristics of a primary (non-rechargeable) battery connected to **VCC** pins should meet the following prerequisites to comply with the module **VCC** requirements summarized in Table 5:

- **Maximum pulse and DC discharge current**: the non-rechargeable battery with its related output circuit connected to the **VCC** pins must be capable of delivering the maximum current consumption occurring during up-link transmissions to the Satellite system, as specified in the SARA-S520BM10 data sheet [1]. The maximum discharge current is not always reported in the data sheets of batteries, but the maximum DC discharge current is typically almost equal to the battery capacity in Amp-hours divided by 1 hour.
- **DC series resistance**: the non-rechargeable battery with its output circuit must be capable of avoiding a VCC voltage drop below the operating range summarized in Table 5 during transmission.

2.2.1.6 Guidelines for external battery charging circuit

SARA-S520BM10 modules do not have an on-board charging circuit. Figure 19 provides an example of a battery charger design, suitable for applications that are Li-Ion (or Li-Pol) battery powered.

In the application circuit, a rechargeable Li-Ion (or Li-Pol) battery cell, that features the correct pulse and DC discharge current capabilities and the appropriate DC series resistance, is directly connected to the **VCC** supply input of the module. Battery charging is completely managed by the battery charger IC, which from a USB power source (5.0 V typ.), linearly charges the battery in three phases:

- **Pre-charge constant current** (active when the battery is deeply discharged): the battery is charged with a low current.
- **Fast-charge constant current**: the battery is charged with the maximum current, configured by the value of an external resistor.
- **Constant voltage**: when the battery voltage reaches the regulated output voltage, the battery charger IC starts to reduce the current until the charge termination is done. The charging process ends when the charging current reaches the value configured by an external resistor or when the charging timer reaches the factory set value.

Using a battery pack with an internal NTC resistor, the battery charger IC can monitor the battery temperature to protect the battery from operating under unsafe thermal conditions.

The battery charger IC, as linear charger, is more suitable for applications where the charging source has a relatively low nominal voltage (~5 V), so that a switching charger is suggested for applications where the charging source has a relatively high nominal voltage (e.g. ~12 V, see section 2.2.1.7 for the specific design-in).

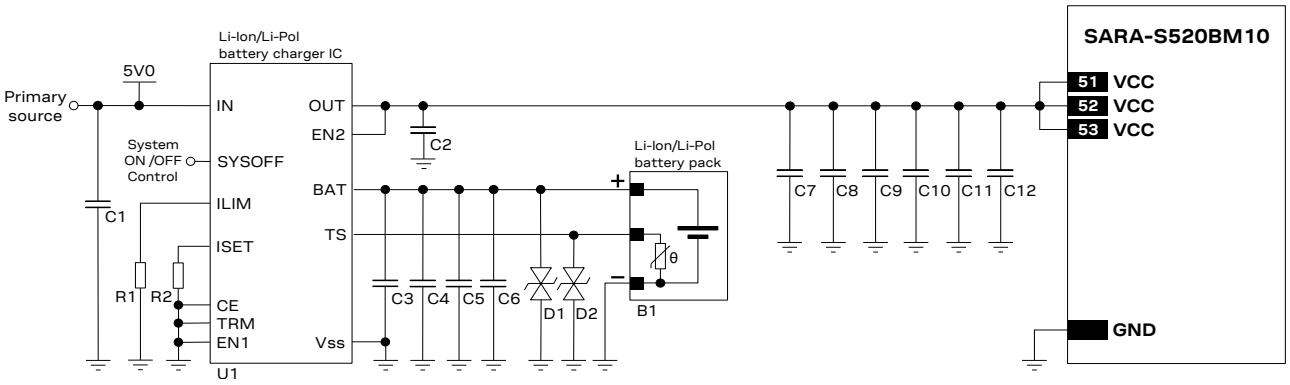

Figure 19: Li-Ion (or Li-Pol) battery charging application circuit

Reference	Description	Part number – Manufacturer
B1	Li-Ion (or Li-Pol) battery pack with NTC	Generic manufacturer
C1, C2, C3	10 µF capacitor ceramic X7R 16 V	Generic manufacturer
C4	100 nF capacitor ceramic X7R 0402 10% 16 V	GCM155R71C104KA55 – Murata
C5	10 nF capacitor ceramic X7R 0402 10% 16 V	GRT155R71C103KE01 – Murata
C6	82 pF capacitor Ceramic C0G 0402 5% 50 V	GRM1555C1H820JA01 – Murata
C7	27 pF capacitor ceramic C0G 0402 5% 50 V	GRM1555C1H270JA01 – Murata
C8	15 pF capacitor ceramic C0G 0402 5% 50 V	GJM1555C1H150JB01 – Murata
C9	330 µF capacitor Tantalum D_SIZE 6.3 V 45 mΩ	T520D337M006ATE045 - KEMET
D1, D2	Low capacitance ESD protection	CG0402MLE-18G – Bourns
R1	1.1 kΩ resistor 0.1 W	Generic manufacturer
R2	1.2 kΩ resistor 0.1 W	Generic manufacturer
U1	Single cell Li-Ion (or Li-Pol) battery charger IC with integrated power path management	BQ24072TR – Texas Instruments

Table 13: Suggested components for the Li-Ion (or Li-Pol) battery charging application circuit

☞ See the section 2.2.1.8, and in particular Figure 22 / Table 15, for the parts recommended to be provided if the application device integrates an internal antenna.

2.2.1.7 Guidelines for external charging and power path management circuit

Application devices where both a permanent primary supply / charging source (e.g. ~12 V) and a rechargeable back-up battery (e.g. 3.7 V Li-Pol) are available at the same time as a possible supply source, should implement a suitable charger / regulator with integrated power path management function to supply the module and the whole device while simultaneously and independently charging the battery.

Figure 20 reports a simplified block diagram circuit showing the working principle of a charger / regulator with integrated power path management function. This component allows the system to be powered by a permanent primary supply source (e.g. ~12 V) using the integrated regulator, which simultaneously and independently recharges the battery (e.g. 3.7 V Li-Pol) that represents the back-up supply source of the system. The power path management feature permits the battery to supplement the system current requirements when the primary supply source is not available or cannot deliver the peak system currents.

A power management IC should meet the following prerequisites to comply with the module **VCC** requirements summarized in Table 5:

- High efficiency internal step-down converter, with characteristics as indicated in section 2.2.1.2
- Low internal resistance in the active path Vout – Vbat, typically lower than 50 mΩ
- High efficiency switch mode charger with separate power path control

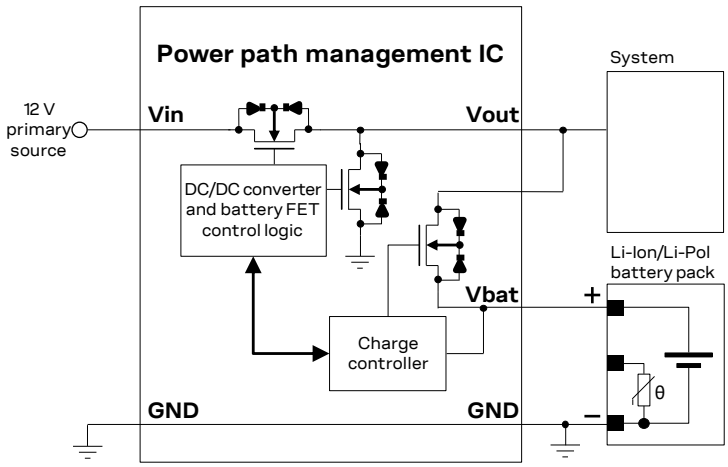

Figure 20: Charger / regulator with integrated power path management circuit block diagram

Figure 21 and the parts listed in Table 14 provide an application circuit example where the MPS MP2617H switching charger / regulator with integrated power path management function provides the supply to the cellular module. At the same time it also concurrently and autonomously charges a suitable Li-Ion (or Li-Pol) battery with the correct pulse and DC discharge current capabilities and the appropriate DC series resistance according to the rechargeable battery recommendations described in section 2.2.1.4.

The MP2617H IC constantly monitors the battery voltage and selects whether to use the external main primary supply / charging source or the battery as supply source for the module, and starts a charging phase accordingly.

The MP2617H IC normally provides a supply voltage to the module regulated from the external main primary source allowing immediate system operation even under missing or deeply discharged battery: the integrated switching step-down regulator is capable to provide up to 3 A output current with low output ripple and fixed 1.6 MHz switching frequency in PWM mode operation. The module load is satisfied in priority, then the integrated switching charger will take the remaining current to charge the battery.

Additionally, the power path control allows an internal connection from battery to the module with a low series internal ON resistance (40 mΩ typical), in order to supplement additional power to the module when the current demand increases over the external main primary source or when this external source is removed.

Battery charging is managed in three phases:

- **Pre-charge constant current** (active when the battery is deeply discharged): the battery is charged with a low current, set to 10% of the fast-charge current
- **Fast-charge constant current**: the battery is charged with the maximum current, configured by the value of an external resistor to a value suitable for the application
- **Constant voltage**: when the battery voltage reaches the regulated output voltage (4.2 V), the current is progressively reduced until the charge termination is done. The charging process ends when the charging current reaches the 10% of the fast-charge current or when the charging timer reaches the value configured by an external capacitor

Using a battery pack with an internal NTC resistor, the MP2617H can monitor the battery temperature to protect the battery from operating under unsafe thermal conditions.

Several parameters as the charging current, the charging timings, the input current limit, the input voltage limit, the system output voltage can be easily set according to the specific application requirements, as the actual electrical characteristics of the battery and the external supply / charging source: suitable resistors or capacitors must be accordingly connected to the related pins of the IC.

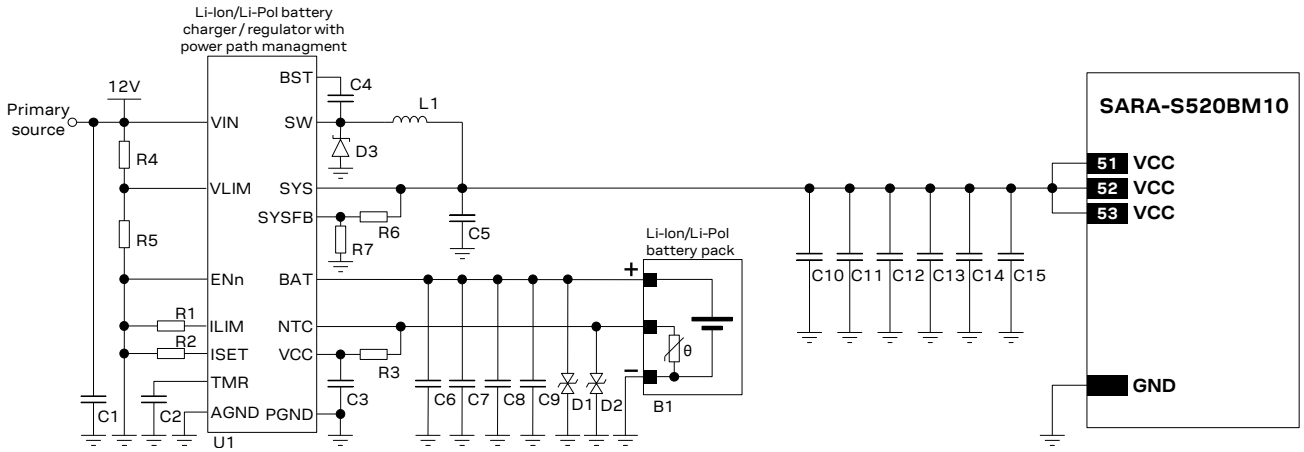

Figure 21: Li-Ion (or Li-Pol) battery charging and power path management application circuit

Reference	Description	Part number – Manufacturer
B1	Li-Ion (or Li-Pol) battery pack with 10 kΩ NTC	Various manufacturer
C1, C5, C6	22 µF capacitor ceramic X5R 0603 10% 25 V	GRM188R60J226MEA0 – Murata
C2, C4, C10	100 nF capacitor ceramic X7R 0402 10% 16 V	GCM155R71C104KA55 – Murata
C3	1 µF capacitor ceramic X7R 0603 10% 25 V	GCM188R71E105KA64 – Murata
C7, C12	82 pF capacitor Ceramic C0G 0402 5% 50 V	GRM1555C1H820JA01 – Murata
C8, C13	27 pF capacitor ceramic C0G 0402 5% 50 V	GRM1555C1H270JA01 – Murata
C9, C14	15 pF capacitor ceramic C0G 0402 5% 50 V	GJM1555C1H150JB01 – Murata
C15	330 µF capacitor Tantalum D_SIZE 6.3 V 45 mΩ	T520D337M006ATE045 - KEMET
C11	10 nF capacitor ceramic X7R 0402 10% 16 V	GRT155R71C103KE01 – Murata
D1, D2	Low capacitance ESD protection	CG0402MLE-18G – Bourns
D3	Schottky diode 40 V 3 A	MBRA340T3G – ON Semiconductor
R1, R3, R5, R7	10 kΩ resistor 0402 1% 1/16 W	Generic manufacturer
R2	1.05 kΩ resistor 0402 1% 0.1 W	Generic manufacturer
R4	22 kΩ resistor 0402 1% 1/16 W	Generic manufacturer
R6	26.5 kΩ resistor 0402 1% 1/16 W	Generic manufacturer
L1	2.2 µH inductor 7.4 A 13 mΩ 20%	SRN8040-2R2Y – Bourns
U1	Li-Ion/Li-Pol battery DC-DC charger / regulator with integrated power path management function	MP2617H – Monolithic Power Systems (MPS)

Table 14: Suggested components for battery charging and power path management application circuit

☞ See the section 2.2.1.8, and in particular Figure 22 / Table 15, for the parts recommended to be provided if the application device integrates an internal antenna.

2.2.1.8 Additional guidelines for VCC supply circuit design

To reduce voltage drops, use a low impedance power source. The series resistance of the supply lines (connected to the modules' **VCC** and **GND** pins) on the application board and battery pack should also be considered and minimized: cabling and routing must be as short as possible to minimize losses.

Three pins are allocated to **VCC** supply connection. Several pins are designated for **GND** connection. It is recommended to correctly connect all of them to supply the module minimizing series resistance.

To reduce voltage ripple and noise, improving RF performance especially if the application device integrates an internal antenna, place the following bypass capacitors near the **VCC** pins:

- 82 pF capacitor with self-resonant frequency in the ~800 MHz frequency range (as the Murata GRM1555C1H820J), to filter EMI in the low cellular frequency bands
- 27 pF capacitor with self-resonant frequency in the ~1600 MHz frequency range (as the Murata GRM1555C1H820J), to filter EMI in the GNSS / Satellite frequency bands
- 15 pF capacitor with self-resonant frequency in the ~1900 MHz frequency range (as the Murata GRM1555C1H150J), to filter EMI in the mid cellular frequency bands
- 10 nF capacitor (e.g. Murata GRM155R71C103K), to filter digital logic noise from clocks and data
- 100 nF capacitor (e.g. Murata GRM155R61C104K), to filter digital logic noise from clocks and data

An additional capacitor with large capacitance (at least 100 µF) and low ESR is recommended to avoid undershoot and overshoot at the start and at the end of RF transmission:

- 330 µF capacitance, 45 mΩ ESR (as the KEMET T520D337M006ATE045)

An additional series ferrite bead may be provided for additional RF noise filtering:

- Ferrite bead specifically designed for EMI / noise suppression in the GHz frequency band (e.g. the Murata BLM18EG221SN1), placed as close as possible to the **VCC** input pins of the module.

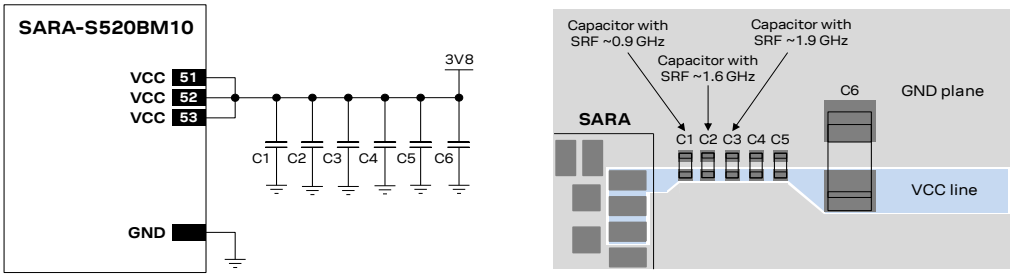

Figure 22: Suggested design to reduce ripple / noise on VCC, particularly suitable when using an integrated antenna

Reference	Description	Part number – Manufacturer
C1	82 pF Capacitor Ceramic C0G 0402 5% 50 V	GRM1555C1H820JA01 – Murata
C2	27 pF capacitor ceramic C0G 0402 5% 50 V	GRM1555C1H270JA16 – Murata
C3	15 pF capacitor ceramic C0G 0402 5% 50 V	GRM1555C1H150JB01 – Murata
C4	10 nF capacitor ceramic X7R 0402 10% 16 V	GRT155R71C103KE01 – Murata
C5	100 nF capacitor ceramic X7R 0402 10% 16 V	GCM155R71C104KA55 – Murata
C6	330 µF Capacitor Tantalum D_SIZE 6.3 V 45 mΩ	T520D337M006ATE045 - KEMET

Table 15: Suggested components to reduce ripple / noise on VCC

☞ The necessity of each part depends on the specific design, but it may be in particular suitable to provide all the parts described in Figure 22 / Table 15 if the device integrates an internal antenna.

☞ ESD sensitivity rating of the **VCC** supply pins is 1 kV (HBM). Higher protection level can be required if the line is externally accessible on the application board, e.g. if accessible battery connector is directly connected to the supply pins. Higher protection level can be achieved by mounting an ESD protection (e.g. EPCOS CA05P4S14THSG varistor) close to accessible point.

2.2.1.9 Guidelines for VCC supply layout design

Good connection of the module **VCC** pins with DC supply source is required for correct RF performance. Guidelines are summarized in the following list:

- All the available **VCC** pins must be connected to the DC source.
- The series resistance along the **VCC** path must be as minimum as possible.
- Any series component with Equivalent Series Resistance (ESR) greater than few milliohms must be avoided.
- **VCC** connection must be routed through a PCB area separated from RF lines / parts, sensitive analog signals and sensitive functional units: it is good practice to interpose at least one layer of PCB ground between the **VCC** track and other signal routing.
- **VCC** connection must be routed as far as possible from the antenna, in particular if embedded in the application device: see Figure 23.
- Coupling between **VCC** and digital lines must be avoided.
- The tank bypass capacitor for current spikes smoothing described in section 2.2.1.8 should be placed close to the **VCC** pins. If the main DC source is a switching DC-DC converter, place the large capacitor close to the DC-DC output and minimize **VCC** track length. Otherwise consider using separate capacitors for DC-DC converter and module.
- The bypass capacitors in the pF range described in Figure 22 and Table 15 should be placed as close as possible to the **VCC** pins, where the **VCC** line narrows close to the module input pins, improving the RF noise rejection in the band centered on the self-resonant frequency of the pF capacitors. This is in particular suitable if the application device integrates an internal antenna.
- Since **VCC** input provides the supply to RF power amplifiers, voltage ripple at high frequency may result in unwanted spurious modulation of transmitter RF signal. This is more likely to happen with switching DC-DC converters, in which case it is better to select the highest operating frequency for the switcher and add a large L-C filter before connecting to the SARA-S520BM10 modules in the worst case.
- Shielding of switching DC-DC converter circuit, or at least the use of shielded inductors for the switching DC-DC converter, may be considered since all switching power supplies may potentially generate interfering signals as a result of high-frequency high-power switching.
- If **VCC** is protected by transient voltage suppressor to ensure that the voltage maximum ratings are not exceeded, place the protecting device along the path from the DC source toward the module, preferably closer to the DC source (otherwise protection function may be compromised).

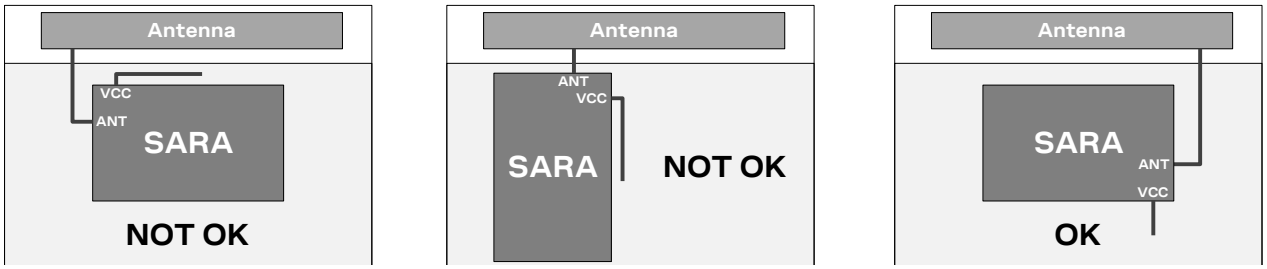

Figure 23: VCC line routing guideline for designs integrating an embedded antenna

2.2.1.10 Guidelines for grounding layout design

Good connection of the module **GND** pins with application PCB solid ground layer is required for correct RF performance. It significantly reduces EMC issues and provides a thermal heat sink for the module.

The specific implementation of the grounding of each **GND** pad defines the thermal heat sink over the related **GND** pad: good grounding of a **GND** pad allows good thermal heat sink over the **GND** pad, and vice versa.

Most of the heat of SARA-S520BM10 modules is generated by the internal Satellite Power Amplifier designed to transmit RF signals at roughly +31.5 dBm output RF power as per ORBCOMM Satellite system specifications. The heat generated by the internal Satellite Power Amplifier needs to be dissipated as much as possible optimizing the ground connection of the **GND** pins of the module located in the related area near the internal Satellite Power Amplifier.

Instead, the internal 26 MHz Temperature-Controlled Crystal Oscillator (TCXO) needs to be isolated as much as possible from thermal heating, making a weak ground connection of the **GND** pins of the module located in the related area near the internal TCXO.

The placement on the top layer of the SARA-S520BM10 modules of the internal TCXO and the internal Satellite Power Amplifier is illustrated in Figure 24, showing also the location of the **GND** pins and the RF pins on the bottom layer of the module.

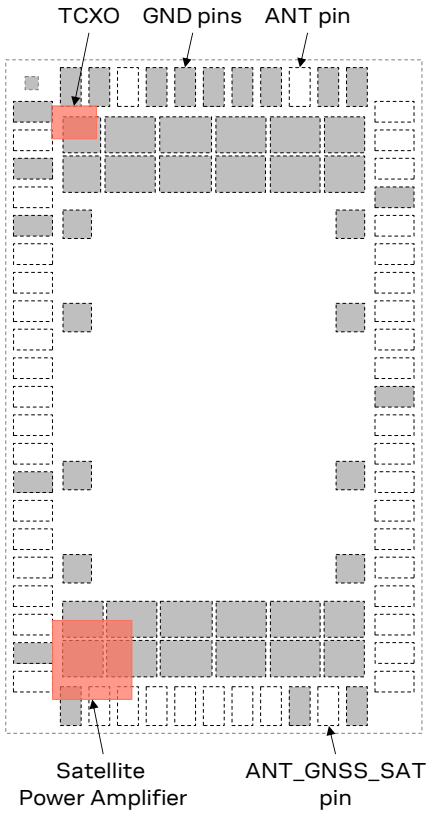

Figure 24: TCXO, Satellite PA, GND and RF pins location on SARA-S520BM10 modules (top view / module through view)

Guidelines for **GND** pins connection are summarized in the following list:

- Provide an optimal ground connection of the **GND** pins in the area where the internal Satellite Power Amplifier is located, increasing as much as possible the number of vias for the GND pins on the application board located in this area down to the application board solid ground layer..
- Provide a weak ground connection of the **GND** pins in the area where the internal TCXO is located.
- Provide one or more dedicated via down to the application board solid ground layer for each **GND** pad surrounding **VCC** pins have.

- The **VCC** supply current flows back to main DC source through GND as ground current: provide adequate return path with suitable uninterrupted ground plane to main DC source.
- Implement one layer of the application PCB as GND plane as wide as possible.
- If the application board is a multilayer PCB, then all the layers should be filled with GND plane as much as possible and each GND area should be connected together with complete via stack down to the main ground layer of the board. Use as many vias as possible to connect the ground planes.
- Provide a dense line of vias at the edges of each GND area, in particular along RF and high-speed lines, and along the edges of the application PCB.
- If the whole application device is composed by more than one PCB, then it is required to provide a good and solid ground connection between the GND areas of all the different PCBs.

2.2.2 Generic digital interfaces supply output (V_INT)

2.2.2.1 Guidelines for V_INT circuit design

SARA-S520BM10 modules provide the **V_INT** generic digital interfaces 1.8 V supply output, which can be mainly used to:

- Indicate when the module is switched on and it is not in the deep-sleep mode or power-off mode
- Supply external devices, as voltage translators, instead of using an external discrete regulator (e.g. see 2.6.1)
- Pull-up SIM detection signal (see section 2.5 for more details)
- Supply GNSS backup domain (see section 2.2.3 for more details)

☞ Do not apply loads which might exceed the maximum available current from **V_INT** supply (see SARA-S520BM10 data sheet [1]) as this can cause malfunctions in internal circuitry.

☞ **V_INT** can only be used as an output: do not connect any external supply source on **V_INT**.

☞ ESD sensitivity rating of the **V_INT** supply pin is 1 kV (HBM according to JESD22-A114). Higher protection level could be required if the line is externally accessible and it can be achieved by mounting an ESD protection (e.g. EPCOS CA05P4S14THSG) close to accessible point.

☞ It is recommended to monitor the **V_INT** pin to sense the end of the internal switch-off sequence of SARA-S520BM10 modules: **VCC** supply can be removed only after **V_INT** goes low.

☞ It is recommended to provide direct access to the **V_INT** pin on the application board by an accessible test point directly connected to the **V_INT** pin.

2.2.2.2 Guidelines for V_INT layout design

V_INT digital interfaces supply output is generated by an integrated switching step-down converter, used internally to supply the digital interfaces. Because of this, it can be a source of noise: avoid coupling with sensitive signals.

2.2.3 GNSS backup supply input (V_BCKP_GNSS)

2.2.3.1 Guidelines for V_BCKP_GNSS circuit design

Power supply at **V_BCKP_GNSS** is optional. If the internal u-blox M10 chipset is switched off, but the **V_BCKP_GNSS** pin is supplied, the receiver enters the hardware backup mode. In this mode, the RTC time and the GNSS orbit data in the BBR are maintained. Valid time and GNSS orbit data at startup improve positioning performance by enabling hot starts and warm starts. Thus, it ensures faster TTFF when the internal u-blox M10 chipset is again switched on.

To make these features always available, connect an independent power supply to **V_BCKP_GNSS** to ensure backup domain supply when the internal u-blox M10 chipset is switched off, as in Figure 25. **V_BCKP_GNSS** pin electrical characteristics are described in the SARA-S520BM10 data sheet [1].

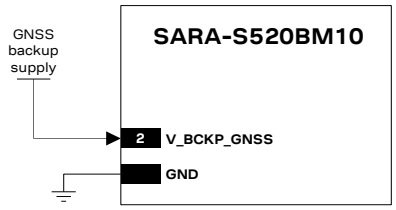

Figure 25: V_BCKP_GNSS application circuit using an independent power supply

Designs using an external battery as a power source at **V_BCKP_GNSS** pin must consider the battery capacity. The GNSS satellite ephemeris data are typically valid for up to 4 hours for hot starts, and up to a few days for warm starts. The current consumption in hardware backup mode is defined in the SARA-S520BM10 data sheet [1].

As an alternative, **V_BCKP_GNSS** pin can be shorted with **V_INT** supply (Figure 26), enabling hardware backup mode as long as the module does not enter deep-sleep mode or does not switch-off.

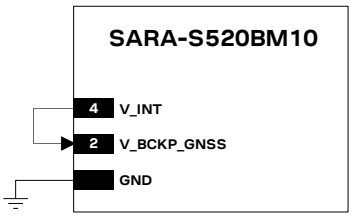

Figure 26: V_BCKP_GNSS application circuit shorting with V_INT supply

To enable the GNSS RTC in hardware backup mode, a 32.768 kHz clock must also be applied (see section 2.10).

Leave **V_BCKP_GNSS** pin unconnected if the GNSS hardware backup mode is not used.

2.2.3.2 Guidelines for V_BCKP_GNSS layout design

The **V_BCKP_GNSS** pin is generally not critical for layout; keep the trace short.

Avoid high resistance on the **V_BCKP_GNSS** line. During the switch to hardware backup mode, a short current adjustment peak may cause a high voltage drop at the pin.

2.3 System functions interfaces

2.3.1 Module power-on (PWR_ON)

2.3.1.1 Guidelines for PWR_ON circuit design

SARA-S520BM10 **PWR_ON** input is equipped with an internal active pull-up resistor; an external pull-up resistor is not required and should not be provided.

If connecting the **PWR_ON** input to a push button, the pin will be externally accessible on the application device. According to EMC/ESD requirements of the application, an additional ESD protection should be provided close to the accessible point, as described in Figure 27 and Table 16.

ESD sensitivity rating of the **PWR_ON** pin is 1 kV (Human Body Model according to JESD22-A114). Higher protection level can be required if the line is externally accessible on the application board, e.g. if an accessible push button is directly connected to **PWR_ON** pin, and it can be achieved by mounting an ESD protection (e.g. EPCOS CA05P4S14THSG varistor) close to the accessible point.

An open drain or open collector output is suitable to drive the **PWR_ON** input from an application processor, as described in Figure 27.

PWR_ON input pin should not be driven high by an external device, as it may cause start up issues.

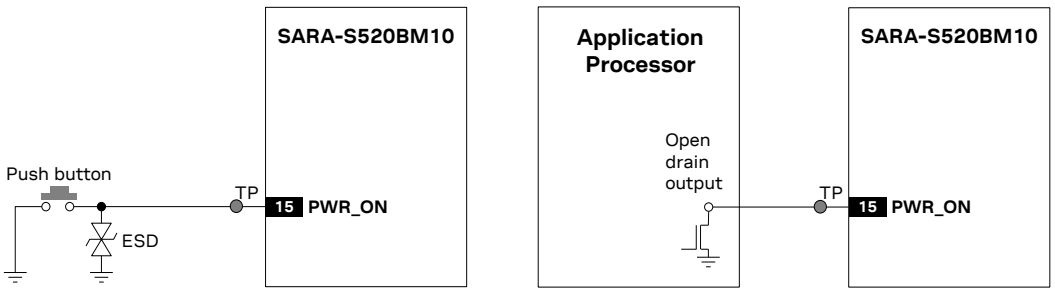

Figure 27: PWR_ON application circuits using a push button and an open drain output of an application processor

Reference	Description	Part number – Manufacturer
ESD	Varistor for ESD protection	B72590T8140S160 – TDK

Table 16: Example ESD protection component for the PWR_ON application circuit

It is recommended to provide direct access to the **PWR_ON** pin on the application board by an accessible test point directly connected to the **PWR_ON** pin.

2.3.1.2 Guidelines for PWR_ON layout design

The power-on circuit (**PWR_ON**) requires careful layout due to the pin function (see sections 1.6.1 and 1.6.2). It is required to ensure that the voltage level is well defined during operation and no transient noise is coupled on this line, otherwise the module might detect a spurious request.

2.3.2 Module reset (RESET_N)

2.3.2.1 Guidelines for RESET_N circuit design

SARA-S520BM10 **RESET_N** is equipped with an internal active pull-up; an external pull-up resistor is not required and should not be provided.

If connecting the **RESET_N** input to a push button, the pin will be externally accessible on the application device. According to EMC/ESD requirements of the application, an additional ESD protection device (e.g. the EPCOS CA05P4S14THSG varistor) should be provided close to accessible point on the line connected to this pin, as described in Figure 28 and Table 17.

☞ ESD sensitivity rating of the **RESET_N** pin is 1 kV (HBM according to JESD22-A114). Higher protection level can be required if the line is externally accessible on the application board, e.g. if an accessible push button is directly connected to the **RESET_N** pin, and it can be achieved by mounting an ESD protection (e.g. EPCOS CA05P4S14THSG varistor) close to accessible point.

An open drain output or open collector output is suitable to drive the **RESET_N** input from an application processor, as described in Figure 28.

☞ **RESET_N** input pin should not be driven high by an external device, as it may cause start up issues.

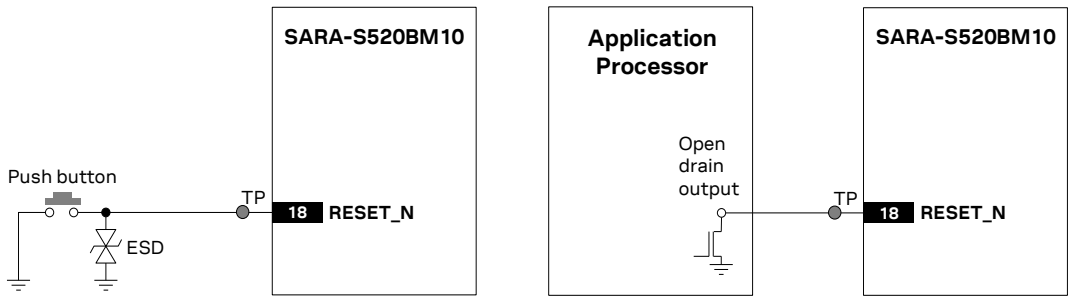

Figure 28: RESET_N application circuits using a push button and an open drain output of an application processor

Reference	Description	Part number – Manufacturer
ESD	Varistor for ESD protection	B72590T8140S160 – TDK

Table 17: Example of ESD protection component for the RESET_N application circuits

☞ If the external reset function is not required by the customer application, the **RESET_N** input pin can be left unconnected to external components, but it is recommended providing direct access on the application board by an accessible test point directly connected to the **RESET_N** input pin.

2.3.2.2 Guidelines for RESET_N layout design

The **RESET_N** circuit require careful layout due to the pin function (see section 1.6.3). Ensure that the voltage level is well defined during operation and no transient noise is coupled on this line, otherwise the module might detect a spurious request. It is recommended to keep the connection line to **RESET_N** pin as short as possible.

2.4 Antenna interfaces

SARA-S520BM10 modules provide the following RF interfaces:

- a cellular RF interface for connecting the external cellular antenna: the **ANT** pin represents the cellular RF input/output for cellular signals transmission and reception.
- the **ANT_GNSS_SAT** pin represents the GNSS RF input of the integrated u-blox M10 concurrent positioning engine and the Satellite Tx output.

The **ANT** and **ANT_GNSS_SAT** pins have a nominal characteristic impedance of 50 Ω and must be connected to the related physical antenna through a 50 Ω transmission line to allow clean transmission / reception of RF signals.

2.4.1 General guidelines for antenna interfaces

2.4.1.1 Guidelines for ANT and ANT_GNSS_SAT pins RF connection design

A clean transition between the **ANT** and **ANT_GNSS_SAT** pads and the application board PCB must be provided, implementing the following design-in guidelines for the layout of the application PCB close to the **ANT** and **ANT_GNSS_SAT** pads:

- On a multilayer board, the whole layer stack below the RF connections should be free of digital lines
- Increase GND keep-out (i.e. clearance, a void area) around the **ANT** and **ANT_GNSS_SAT** pads, on the top layer of the application PCB, to at least 250 µm up to adjacent pads metal definition and up to 400 µm on the area below the module, to reduce parasitic capacitance to ground, as described in the left picture in Figure 29
- Add GND keep-out (i.e. clearance, a void area) on the buried metal layer below the **ANT** and **ANT_GNSS_SAT** pads if the top-layer to buried layer dielectric thickness is below 200 µm, to reduce parasitic capacitance to ground, as described in the right picture in Figure 29

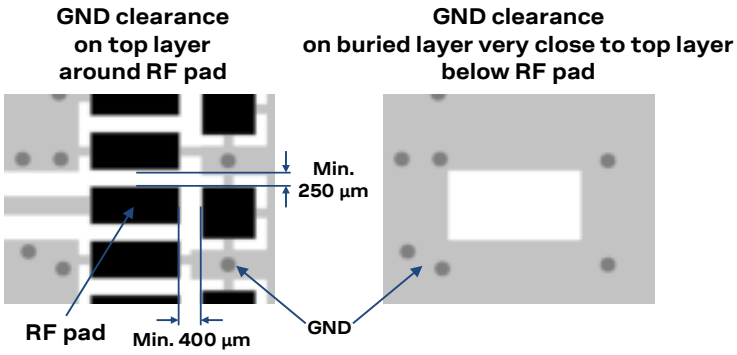

Figure 29: GND keep-out area on top layer around RF pad and on closely buried layer below RF pad (ANT / ANT_GNSS_SAT)

2.4.1.2 Guidelines for RF transmission lines design

Any RF transmission line, such as the ones from the **ANT** and **ANT_GNSS_SAT** pads up to the related antenna connector or up to the related internal antenna pad, must be designed so that the characteristic impedance is as close as possible to 50 Ω.

RF transmission lines can be designed as a micro strip (consists of a conducting strip separated from a ground plane by a dielectric material) or a strip line (consists of a flat strip of metal which is sandwiched between two parallel ground planes within a dielectric material). The micro strip, implemented as a coplanar waveguide, is the most common configuration for printed circuit board.

Figure 30 and Figure 31 provide two examples of suitable 50 Ω coplanar waveguide designs. The first example of RF transmission line can be implemented in case of 4-layer PCB stack-up herein described, and the second example of RF transmission line can be implemented in case of 2-layer PCB stack-up herein described.

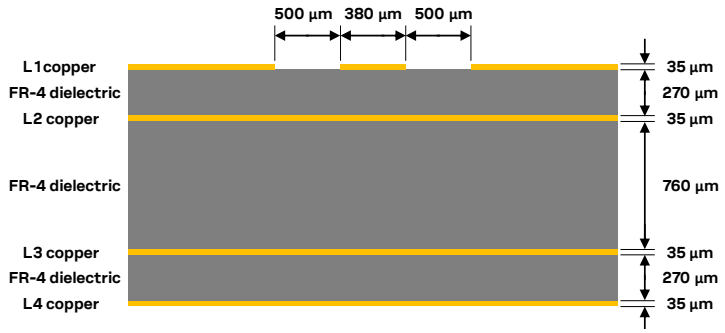

Figure 30: Example of 50 Ω coplanar waveguide transmission line design for the described 4-layer board layup

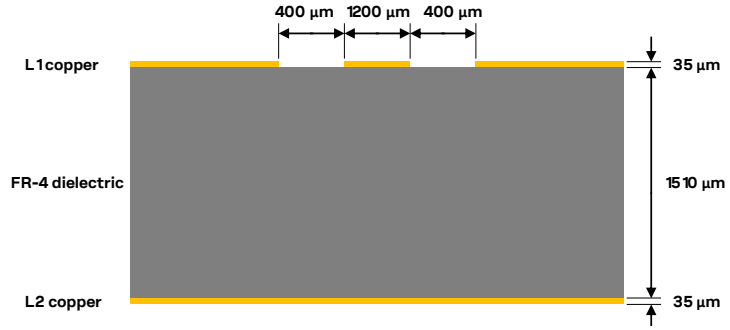

Figure 31: Example of 50 Ω coplanar waveguide transmission line design for the described 2-layer board layup

If the two examples do not match the application PCB stack-up, then the 50 Ω characteristic impedance calculation can be made using the HFSS commercial finite element method solver for electromagnetic structures from Ansys Corporation, or using freeware tools like Avago / Broadcom AppCAD (https://www.broadcom.com/appcad) taking care of the approximation formulas used by the tools for the impedance computation.

To achieve a 50 Ω characteristic impedance, the transmission line width must be chosen due to:

- the thickness of the transmission line itself (e.g. 35 µm in the example of Figure 30 and Figure 31)
- the thickness of the dielectric material between the top layer (where the line is routed) and the inner closer layer implementing the ground plane (e.g. 270 µm in Figure 30, 1510 µm in Figure 31)
- the dielectric constant of the dielectric material (e.g. dielectric constant of the FR-4 dielectric material in Figure 30 and Figure 31)
- the gap from the transmission line to the adjacent ground plane on the same layer of the transmission line (e.g. 500 µm in Figure 30, 400 µm in Figure 31)

If the distance between the transmission line and the adjacent GND area (on the same layer) does not exceed 5 times the width of the line, use the “Coplanar Waveguide” model for the 50 Ω calculation.

Additionally to the 50 Ω impedance, the following guidelines are recommended for transmission lines:

- Minimize the transmission line length: the insertion loss should be minimized as much as possible, in the order of a few tenths of a dB,
- Add GND keep-out (i.e. clearance, a void area) on buried metal layers below any pad of component present on the RF transmission lines, if top-layer to buried layer dielectric thickness is below 200 µm, to reduce parasitic capacitance to ground,
- The transmission lines width and spacing to GND must be uniform and routed as smoothly as possible: avoid abrupt changes of width and spacing to GND,
- Add GND stitching vias around transmission lines, as described in Figure 32,

- Ensure solid metal connection of the adjacent metal layer on the PCB stack-up to main ground layer, providing enough vias on the adjacent metal layer, as described in Figure 32,
- Route RF transmission lines far from any noise source (as switching supplies and digital lines) and from any sensitive circuit (as USB),
- Avoid stubs on the transmission lines,
- Avoid signal routing in parallel to transmission lines or crossing the transmission lines on buried metal layer,
- Do not route microstrip lines below discrete component or other mechanics placed on top layer

Two examples of a suitable RF circuit design for **ANT** pin are illustrated in Figure 32, where the cellular antenna detection circuit is not implemented (if the cellular antenna detection function is required by the application, follow the guidelines for circuit and layout implementation detailed in section 2.4.5):

- In the first example shown on the left, the **ANT** pin is directly connected to an SMA connector by a suitable 50 Ω transmission line, designed with the appropriate layout.
- In the second example shown on the right, the **ANT** pin is connected to an SMA connector by a suitable 50 Ω transmission line, designed with the appropriate layout, with an additional high pass filter to improve the ESD immunity at the antenna port. (The filter consists of a suitable series capacitor and shunt inductor, for example the Murata GRM1555C1H150JB01 15 pF capacitor and the Murata LQG15HN39NJ02 39 nH inductor with SRF ~1 GHz.).

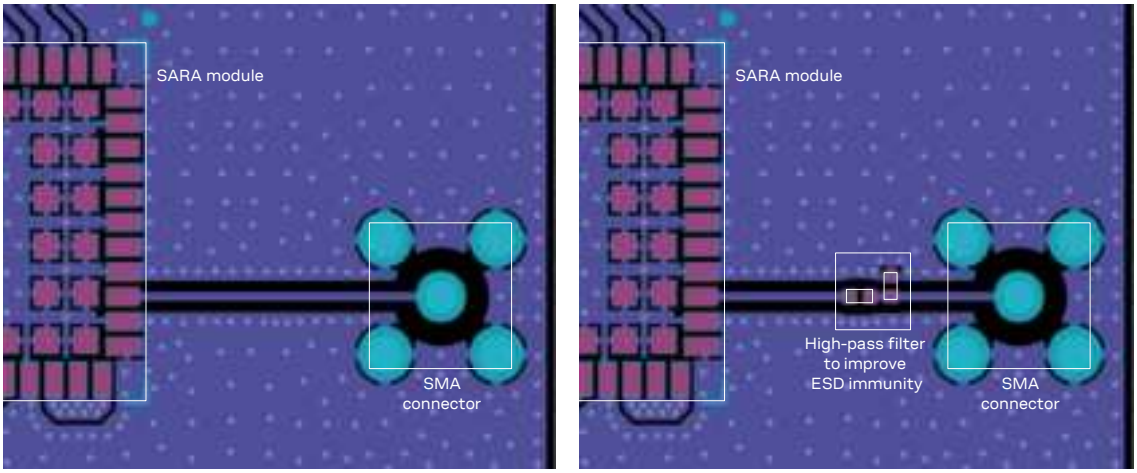

Figure 32: Example of circuit and layout for ANT RF circuits on the application board

2.4.1.3 Guidelines for RF termination design

The RF termination must provide a characteristic impedance of 50 Ω as well as the RF transmission line up to the RF termination, to match the characteristic impedance of **ANT** and **ANT_GNSS_SAT** ports.

However, real antennas do not have a perfect 50 Ω load on all the supported frequency bands. So to reduce as much as possible any performance degradation due to antenna mismatching, the RF termination must provide optimal return loss (or VSWR) figures over all the operating frequencies, as summarized in Table 6 and Table 7.

If an external antenna is used, the antenna connector represents the RF termination on the PCB:

- Use a suitable 50 Ω connector providing a clean PCB-to-RF-cable transition.
- Strictly follow the connector manufacturer's recommended layout, for example:
    - SMA Pin-Through-Hole connectors require a GND keep-out (i.e. clearance, a void area) on all the layers around the central pin up to the annular pads of the four GND posts, as illustrated in Figure 32.

- U.FL surface mounted connectors require no conductive traces (i.e. clearance, a void area) in the area below the connector between the GND land pads, as illustrated in Figure 33.

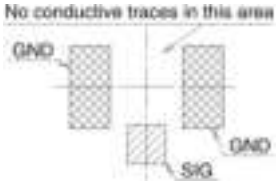

Figure 33: U.FL surface mounted connector mounting pattern layout

- Cut out the GND layer under the RF connector and close to any buried vias, to remove stray capacitance and thus keep the RF line at 50 Ω, e.g. the active pad of U.FL connector needs to have a GND keep-out (i.e. clearance, a void area) at least on the first inner layer to reduce parasitic capacitance to ground.

If an integrated antenna is used, the integrated antenna represents the RF terminations. The following guidelines should be followed:

- Use an antenna designed by an antenna manufacturer providing the best possible return loss.
- Provide a ground plane large enough according to the relative integrated antenna requirements. The ground plane of the application PCB can be reduced down to a minimum size that must be similar to one quarter of wavelength of the minimum frequency that needs to be radiated. As numerical example,
  Frequency = 617 MHz → Wavelength ≅ 48 cm → Minimum GND plane size ≅ 12 cm
- It is highly recommended to strictly follow the detailed and specific guidelines provided by the antenna manufacturer regarding correct installation and deployment of the antenna system, including the PCB layout and matching circuitry.
- Further to the custom PCB and product restrictions, the antenna may require a tuning to comply with all the applicable required certification schemes. It is recommended to consult the antenna manufacturer for antenna matching design-in guidelines relative to the custom application.

Additionally, these recommendations regarding the antenna system placement must be followed:

- Do not place the antennas within a closed metal case.
- Do not place the cellular antenna in close vicinity to the end user since the emitted radiation in human tissue is restricted by regulatory requirements.
- Place the antennas as far as possible from VCC supply line and related parts (see also Figure 23), from high speed digital lines (as USB) and from any possible noise source.
- Place the antenna far from sensitive analog systems or employ countermeasures to reduce EMC or EMI issues.
- Be aware of interaction between co-located RF systems since the LTE transmitted power may interact or disturb the performance of companion systems (see also section 2.4.4).

2.4.2 Cellular antenna RF interface (ANT)

2.4.2.1 Guidelines for antenna selection and design

The antenna is the most critical component to be evaluated. Designers must take care of the antenna from all perspective at the very start of the design phase when the physical dimensions of the application board are under analysis/decision, since the cellular compliance of the device integrating SARA-S520BM10 modules with all the applicable required certification schemes depends on antenna's radiating performance.

Cellular antennas are typically available as:

- External antennas (e.g. linear monopole):
  - External antennas basically do not imply physical restriction to the design of the PCB where the SARA-S520BM10 module is mounted.
  - The radiation performance mainly depends on the antennas. It is required to select antennas with optimal radiating performance in the operating bands.
  - RF cables should be carefully selected to have minimum insertion losses. Additional insertion loss will be introduced by low quality or long cable. Large insertion loss reduces both transmit and receive radiation performance.
  - A high quality 50 Ohm RF connector provides a clean PCB-to-RF-cable transition. It is recommended to strictly follow the layout and cable termination guidelines provided by the connector manufacturer.
- Integrated antennas (e.g. PCB antennas such as patches or ceramic SMT elements):
  - Internal integrated antennas imply physical restriction to the design of the PCB: integrated antenna excites RF currents on its counterpoise, typically the PCB ground plane of the device that becomes part of the antenna: its dimension defines the minimum frequency that can be radiated. Therefore, the ground plane can be reduced to a minimum size that should be similar to the quarter of the wavelength of the minimum frequency that needs to be radiated, given that the orientation of the ground plane relative to the antenna element must be considered. As numerical example, the physical restriction to PCB design can be considered as following:
    Frequency = 617 MHz → Wavelength ≅ 48 cm → Minimum GND plane size ≅ 12 cm
  - Radiation performance depends on the whole PCB and antenna system design, including product mechanical design and usage. Antennas should be selected with optimal radiating performance in the operating bands according to the mechanical specifications of the PCB and the whole product.
  - It is recommended to select a custom antenna designed by an antennas' manufacturer if the required ground plane dimensions are very small (e.g. less than 6.5 cm long and 4 cm wide). The antenna design process should begin at the start of the whole product design process.
  - It is highly recommended to strictly follow the detailed and specific guidelines provided by the antenna manufacturer regarding correct installation and deployment of the antenna system, including PCB layout and matching circuitry.
  - Further to the custom PCB and product restrictions, antennas may require tuning to obtain the required performance for compliance with all the applicable required certification schemes. It is recommended to consult the antenna manufacturer for the design-in guidelines for antenna matching relative to the custom application.

In both of cases, selecting external or internal antennas, these recommendations should be observed:

- Select an antenna providing optimal return loss / VSWR / efficiency figure over all the operating cellular frequencies.
- Select an antenna providing the worst possible return loss / VSWR / efficiency figure in the GNSS frequency band, to optimize the RF coexistence between the cellular and the GNSS systems (see section 2.4.4 for further details and guidelines regarding cellular / GNSS RF coexistence).
- Select an antenna providing appropriate gain figure (i.e. combined directivity and efficiency figure) so that the RF radiation intensity do not exceed the regulatory limits specified in some countries: refer to the FCC United States notice reported in section 4.2, the ISED Canada notice reported in section 4.3, the CE notice for Europe reported in section 4.4, etc.

☞ For examples of antennas intended to be surface-mounted on the device integrating the module, examples of antennas with cable and connector intended to be placed off-board inside the device integrating the module, and examples of antennas intended to be mounted outside the device integrating the module, please contact the u-blox office or sales representative nearest you.

2.4.3 GNSS / Satellite antenna RF interface (ANT_GNSS_SAT)

As indicated in the ORBCOMM conformity section 4.5, to launch a product onto satellite networks, the product integrating the SARA-S520BM10 module requires a Type Approval certificate from ORBCOMM satellite network operator.

If the final product integrating the SARA-S520BM10 module uses one of the ORBCOMM-specified antennas, without any change in the antenna or cable, the ORBCOMM Type Approval process will be granted in a simplified process (the so-called green line process).

☞ We recommend contacting ORBCOMM to get the list of pre-certified Satellite antennas specified by ORBCOMM for the Satellite RF operations.

2.4.3.1 Guidelines for applications with a GNSS / Satellite passive antenna

If an external GNSS / Satellite passive antenna is used, as one of the ORBCOMM-specified antennas, the example of circuit illustrated in Figure 34 can be implemented.

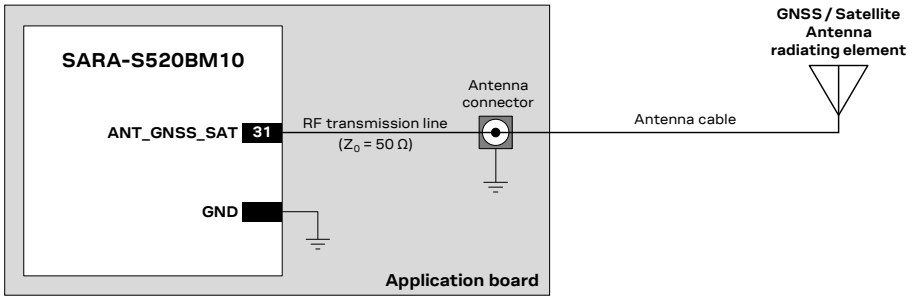

Figure 34: Minimum circuit with GNSS / Satellite passive antenna

The antenna and its placement are critical system factors for accurate GNSS / Satellite RF signals reception. We recommend placing the GNSS / Satellite antenna radiating element in a position with a good sky view, and as far as possible from any possible source of noise.

2.4.3.2 Guidelines for applications with a GNSS / Satellite active antenna

If an external GNSS / Satellite antenna with LNA included in the GNSS and/or Satellite receiving RF path is used, the external LNA(s) can be enabled / disabled using the Satellite / GNSS Rx indication function available on the GPIO pin of SARA-S520BM10 modules as illustrated in section 1.11.

Additionally, the Tx / Rx RF path of the external RF antenna system, and/or the GNSS / Satellite RF path of the external RF antenna system can be selected with appropriate RF switch(es) controlled by the Satellite / GNSS Tx / Rx indication and the Satellite / GNSS Rx indication functions available on the GPIO pins of SARA-S520BM10 modules as illustrated in section 1.11.

2.4.4 Cellular and GNSS RF coexistence

Overview

SARA-S520BM10 modules allow GNSS RF signals reception concurrently with the Cellular LTE RF signals transmission and reception, and with Satellite RF signals reception. Instead, GNSS RF signals reception is not available concurrently with Satellite RF signals transmission.

Desensitization or receiver blocking is a form of electromagnetic interference (EMI) where a radio receiver is unable to detect a weak signal that it might otherwise be able to receive when there is no interference (see Figure 35). Good blocking performance is particularly important in the scenarios where several radios of various forms are used in close proximity to each other.

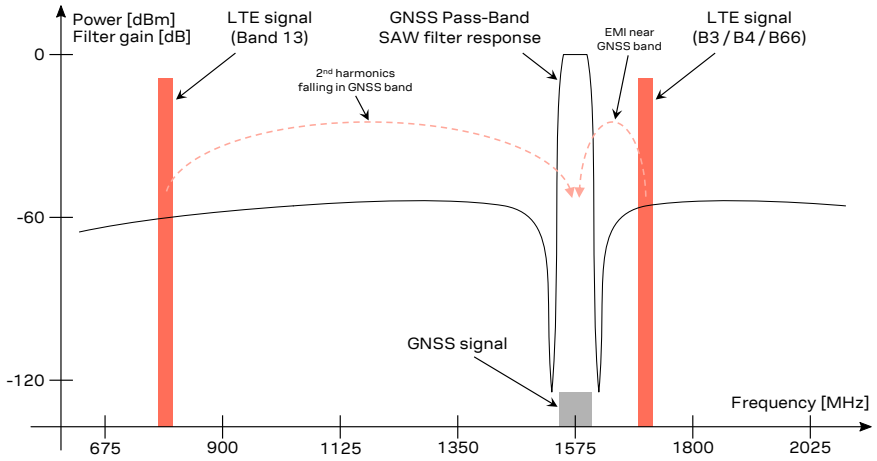

Figure 35: EMI due to Tx in LTE B3, B4, B66 low channels (1710 MHz) adjacent to GNSS frequency range (1559 to 1610 MHz), or due to Tx in LTE B13 high channels (787 MHz) with harmonics falling into the GNSS frequency range

Jamming signals may come from in-band and out-band frequency sources. In-band jamming is caused by signals with frequencies falling within the GNSS frequency range, while out-band jamming is caused by very strong signals with frequencies adjacent to the GNSS frequency range so that part of the strong signal power may leak at the input of the GNSS receiver and/or block GNSS reception.

If not properly taken into consideration, in-band and out-band jamming signals may cause a reduction in the carrier-to-noise power density ratio (C/No) of the GNSS satellites.

In-band interference

In-band interference signals are typically caused by harmonics from displays, switching converters, micro-controllers and bus systems. Moreover, considering for example the LTE band 13 high channel transmission frequency (787 MHz) and the GPS operating band (1575.42 MHz ± 1.023 MHz), the second harmonic of the cellular signal is exactly within the GPS operating band. Therefore, depending on the board layout and the transmit power, the highest channel of LTE band 13 is the channel that has the greatest impact on the C/No reduction.

Countermeasures against in-band interference include:

- Maintaining a good grounding concept in the design,
- Ensuring proper shielding of the different RF paths,
- Ensuring proper impedance matching of RF traces,
- Placing the GNSS antenna away from noise sources,
- Add a notch filter along the GNSS RF path, just after the antenna, at the frequency of the jammer

Out-of-band interference

Out-band interference is caused by signal frequencies that are different from the GNSS, the main sources being cellular, Wi-Fi, bluetooth transmitters, etc. For example, the lowest channels in LTE band 3, 4 and 66 can compromise the good reception of the GLONASS satellites. Again, the effect can be explained by comparing the LTE frequencies (low channels transmission frequency is 1710 MHz) with the GLONASS operating band (1602 MHz ± 8 MHz). In this case the LTE signal is outside the useful GNSS band, but, provided that the power received by the GNSS subsystem at 1710 MHz is high enough, blocking and leakage effects may appear reducing once again the C/No.

Countermeasures against out-band interference include:

- Maintaining a good grounding concept in the design,
- Keeping the GNSS and cellular antennas more than the quarter-wavelength (of the minimum Tx frequency) away from each other; if for layout or size reasons this requirement cannot be met, then the antennas should be placed orthogonally to each other and/or on different side of the PCB,
- Selecting a cellular antenna providing the worst possible return loss / VSWR / efficiency figure in the GNSS frequency band: the lower is the cellular antenna efficiency between 1559 MHz and 1610 MHz, the higher is the isolation between the cellular and the GNSS systems,
- Ensuring at least 15 – 20 dB isolation between antennas in the GNSS band by implementing the most suitable placement for the antennas, considering the related radiation diagrams of the antennas: better isolation results from antenna patterns with radiation lobes in different directions considering the GNSS frequency band.

Countermeasures for small devices

Implementing all the countermeasures mentioned above, in particular ensuring appropriate isolation, may be difficult in application devices with very small dimensions, so that adding an external GNSS stop-band SAW filter along the cellular RF line has to be considered to optimize the RF coexistence.

The GNSS stop-band SAW filter shall provide very low attenuation in the cellular frequency bands (see Table 18 for possible suitable examples) to avoid affecting cellular TRP and/or TIS RF performances. Adding an external GNSS stop-band SAW filter along the cellular RF line has to be carefully evaluated according to specific application requirements regarding Cellular and GNSS RF coexistence, as the additional insertion loss of such filter may affect the cellular TRP and/or TIS RF figures.

Manufacturer	Part number	Description
Qualcomm RF360	B8666	GNSS (L1) SAW extractor filter, 1.7 x 1.3 mm
Qualcomm RF360	B8939	GNSS (L1) SAW extractor filter, 1.5 x 1.1 mm
Murata	SADAC1G56AB0E0A	GNSS (L1) SAW extractor filter, 1.5 x 1.1 mm
TST	TE0123A	GPS (1575.42 MHz) SAW band-stop filter, 3.0 x 3.0 mm

Table 18: Examples of GNSS band-stop SAW filters

Additional considerations

The interference of a cellular transmitter depends on the actual Tx power level of the cellular RF signal. An interference visible at maximum Tx power level may be negligible at medium/low Tx power levels. Similarly, the interference may be negligible in case the cellular transmission lasts for short time.

Note that high-power transmission occurs very infrequently on a live network according to the Tx power distribution data shown in the GSMA official document TS.09 [10]. Additionally, typical LTE-M and/or NB-IoT applications usually implement transmission of few data, lasting very short in time. Therefore, depending on the application, careful PCB layout, antenna selection and placement should be sufficient to ensure accurate GNSS reception.

2.4.5 Cellular antenna detection interface (ANT_DET)

2.4.5.1 Guidelines for ANT_DET circuit design

Figure 36 and Table 19 describe the recommended schematic / components for the cellular antenna detection circuit to be provided on the application board and for the diagnostic circuit that must be provided on the antenna's assembly to achieve antenna detection functionality.

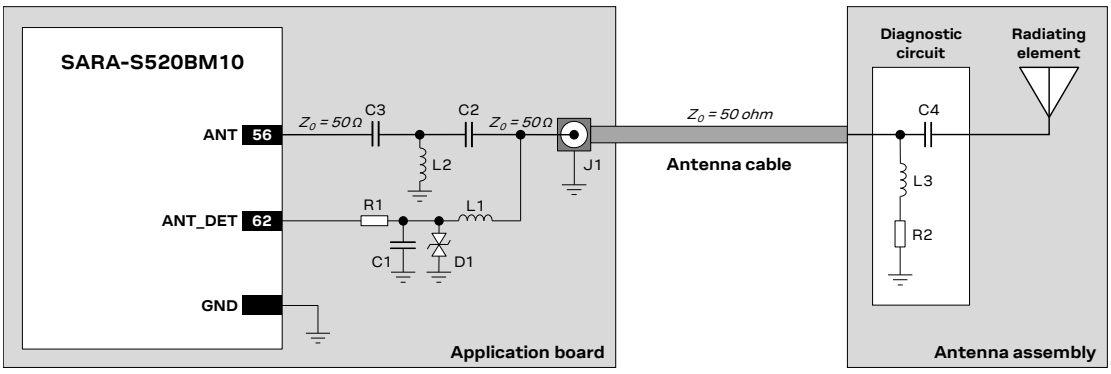

Figure 36: Suggested schematic for antenna detection circuit on application PCB and diagnostic circuit on antenna assembly

Reference	Description	Part number – Manufacturer
C1	27 pF capacitor ceramic C0G 0402 5% 50 V	GRM1555C1H270JA16 – Murata
C2	33 pF capacitor ceramic C0G 0402 5% 50 V	GRM1555C1H330JA16 – Murata
D1	Very low capacitance ESD protection	PESD0402-140 – Tyco Electronics
L1	68 nH multilayer inductor 0402 (SRF ~1 GHz)	LQG15HS68NJ02 – Murata
R1	10 kΩ resistor 0402 1% 0.063 W	Generic manufacturer
J1	SMA connector 50 Ω through hole jack	SMA6251A1-3GT50G-50 – Amphenol
C3	15 pF capacitor ceramic C0G 0402 5% 50 V	GRM1555C1H150J – Murata
L2	39 nH multilayer inductor 0402 (SRF ~1 GHz)	LQG15HN39NJ02 – Murata
C4	22 pF capacitor Ceramic C0G 0402 5% 25 V	GCM1555C1H270JA16 – Murata
L3	68 nH multilayer inductor 0402 (SRF ~1 GHz)	LQG15HS68NJ02 – Murata
R2	15 kΩ resistor for diagnostics	Generic manufacturer

Table 19: Suggested parts for antenna detection circuit on application PCB and diagnostic circuit on antennas assembly

The antenna detection and diagnostic circuit suggested in Figure 36 and Table 19 are here explained:

- When antenna detection is forced by the +UANTR AT command (see AT commands manual [2]), the **ANT_DET** pin generates a DC current measuring the resistance (R2) from the antenna connector (J1) provided on the application board to GND.
- DC blocking capacitors are needed at the **ANT** pin (C2) and at the antenna radiating element (C4) to decouple the DC current generated by the **ANT_DET** pin.
- Choke inductors with a Self-Resonance Frequency (SRF) in the range of 1 GHz are needed in series at the **ANT_DET** pin (L1) and in series at the diagnostic resistor (L3), to avoid a reduction of the RF performance of the system, improving the RF isolation of the load resistor.
- Resistor on the **ANT_DET** path (R1) is needed for accurate measurements through the +UANTR AT command. It also acts as an ESD protection.
- Additional components (C1 and D1 in Figure 36) are needed at the **ANT_DET** pin as ESD protection.
- Additional high pass filter (C3 and L2 in Figure 36) is provided as ESD immunity improvement
- The **ANT** pin must be connected to the antenna connector by a transmission line with nominal characteristics impedance as close as possible to 50 Ω.

The DC impedance at RF port for some antennas may be a DC open (e.g. linear monopole) or a DC short to reference GND (e.g. PIFA antenna). For those antennas, without the diagnostic circuit of Figure 36, the measured DC resistance is always at the limits of the measurement range (respectively open or short), and there is no mean to distinguish between a defect on antenna path with similar characteristics (respectively: removal of linear antenna or RF cable shorted to GND for PIFA antenna).

Furthermore, any other DC signal injected to the RF connection from ANT connector to radiating element will alter the measurement and produce invalid results for antenna detection.

☞ It is recommended to use an antenna with a built-in diagnostic resistor in the range from 5 kΩ to 30 kΩ to assure good antenna detection functionality and avoid a reduction of module RF performance. The choke inductor should exhibit a parallel Self-Resonance Frequency (SRF) in the range of 1 GHz to improve the RF isolation of load resistor.

For example:

Consider an antenna with built-in DC load resistor of 15 kΩ. Using the +UANTR AT command, the module reports the resistance value evaluated from the antenna connector provided on the application board to GND:

- Reported values close to the used diagnostic resistor nominal value (i.e. values from 13 kΩ to 17 kΩ if a 15 kΩ diagnostic resistor is used) indicate that the antenna is correctly connected.
- Values close to the measurement range maximum limit or an open-circuit “over range” report (see the AT commands manual [2]) means that the antenna is not connected or the RF cable is broken.
- Reported values below the measurement range minimum limit highlights a short to GND at antenna or along the RF cable.
- Measurement inside the valid measurement range and outside the expected range may indicate an unclean connection, a damaged antenna or incorrect value of the antenna load resistor for diagnostics.
- Reported value could differ from the real resistance value of the diagnostic resistor mounted inside the antenna assembly due to antenna cable length, antenna cable capacity and the used measurement method.

☞ If the antenna detection function is not required by the customer application, the **ANT_DET** pin can be left unconnected and the **ANT** pin can be directly connected to the antenna connector by a 50 Ω transmission line as described in Figure 32.

2.4.5.2 Guidelines for ANT_DET layout design

Figure 37 describes the recommended layout for the cellular antenna detection circuit to be provided on the application board to achieve antenna detection functionality, implementing the recommended schematic described in the previous Figure 36 and Table 19:

- The **ANT** pin must be connected to the cellular antenna connector by a 50 Ω transmission line, implementing the design guidelines described in section 2.4.2 and the recommendations of the SMA connector manufacturer.
- DC blocking capacitor at **ANT** pin (C2) must be placed in series to the 50 Ω RF line.
- The **ANT_DET** pin must be connected to the 50 Ω transmission line by a sense line.
- Choke inductor in series at the **ANT_DET** pin (L1) must be placed so that one pad is on the 50 Ω transmission line and the other pad represents the start of the sense line to the **ANT_DET** pin.
- The additional components (R1, C1, D1) on the **ANT_DET** line must be placed as ESD protection
- The additional high pass filter (C3 and L2) on the **ANT** line is placed as ESD immunity improvement

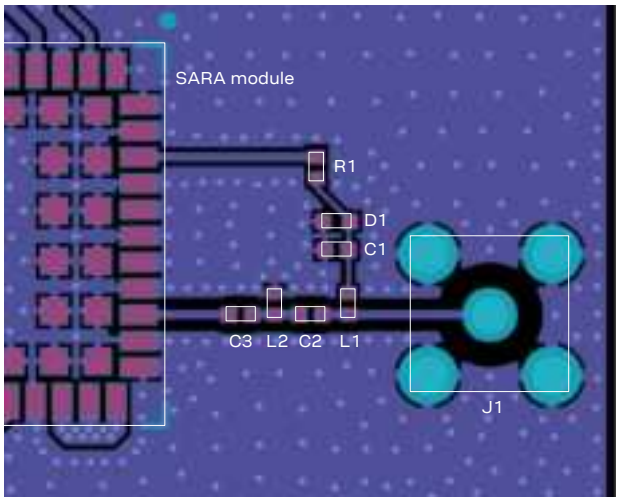

Figure 37: Suggested layout for antenna detection circuit on application board

2.4.6 Cellular antenna dynamic tuning control interface

SARA-S520BM10 modules support a wide range of frequencies, from 600 MHz to 2200 MHz. To provide more efficient antenna designs over a wide bandwidth, **RFCTRL1** and **RFCTRL2** pins can be configured to change their output value in real time according to the operating LTE band in use by the module.

These pins, paired with an external antenna tuner IC or RF switch, can be used to:

- Tune antenna impedance to reduce power losses due to mismatch,
- Tune antenna aperture to improve total antenna efficiency,
- Select the optimal antenna for each operating band

Table 10 reports the antenna dynamic tuning pins setting at the related module operating band.

Figure 38 shows examples of application circuits implementing impedance tuning and aperture tuning. The module controls an RF switch which is responsible for selecting the appropriate matching element for the operating band. Table 20 reports suggested components implementing the SP4T RF switch functionality.

In Figure 38(a), tuning the antenna impedance optimizes the power delivered into the antenna by dynamically adjusting the RF impedance seen by **ANT** pin of SARA-S520BM10 module. By creating a tuned matching network for each operating band, the total radiated power (TRP) and the total isotropic sensitivity (TIS) metrics are improved.

In Figure 38(b), antenna aperture tuning enables higher antenna efficiency over a wide frequency range. The dynamically tunable components are added to the antenna structure itself, thereby modifying the effective electrical length of the radiating element. Thus the resonant frequency of the antenna is shifted into the module's operating frequency band. Aperture tuning optimizes radiation efficiency, insertion loss, isolation, and rejection levels of the antenna.

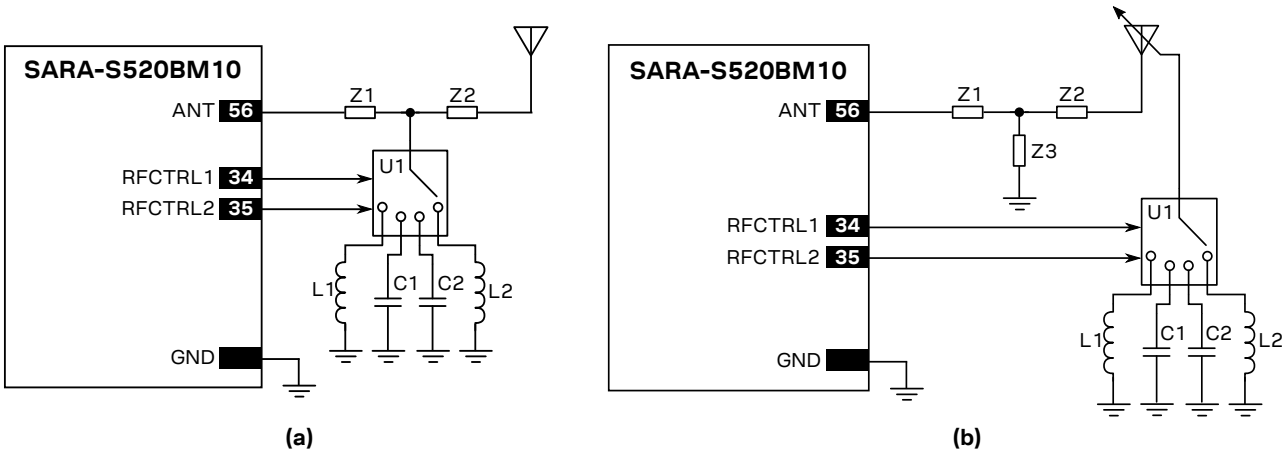

Figure 38: Examples of schematics for cellular antenna dynamic impedance tuning (a) and aperture tuning (b).

☞ Refer to the antenna datasheet and/or manufacturer for proper values of matching components Z1, Z2, Z3, L1, L2, C1, C2. These components should have low losses to avoid degrading the radiating efficiency of the antenna, thereby hindering the positive effects of dynamic tuning.

Manufacturer	Part number	Description
Peregrine Semiconductor	PE42442	30..6000 MHz UltraCMOS SP4T RF switch
Peregrine Semiconductor	PE613050	5..3000 MHz UltraCMOS SP4T RF switch
Peregrine Semiconductor	PE42440	50..3000 MHz UltraCMOS SP4T RF switch
Skyworks Solutions	SKY13626-685LF	400..3800 MHz SP4T high-power RF switch
Skyworks Solutions	SKY13380-350LF	20..3000 MHz SP4T high-power RF switch
KYOCERA AVX	EC646	100..3000 MHz ultra-small SP4T RF switch
KYOCERA AVX	EC686-3	100..3000 MHz ultra-low R_{ON} SP4T RF switch
Qorvo	RF1654A	100..2700 MHz SP4T RF switch
Infineon	BGSA14GN10	100..6000 MHz SP4T RF switch for antenna tuning applications

Table 20: Examples of RF switches for cellular antenna dynamic tuning

2.4.7 Antenna trace design used for module type approvals

The conformity assessment of SARA-S520BM10 LGA surface-mounted modules for regulatory type approvals such as FCC United States, ISED Canada, RED Europe, etc. has been carried out with the modules mounted on a u-blox host printed circuit board with two 50 Ω grounded coplanar waveguide designed on it, herein referenced as “antenna trace design”, implementing the connection from the **ANT** pad of the module up to a 50 Ω SMA connector for external LTE cellular antenna and/or RF cable access, and from the **ANT_GNSS_SAT** pad of the module up to a 50 Ω SMA connector for external Satellite antenna and/or RF cable access.

☞ Manufacturers of mobile or fixed devices incorporating SARA-S520BM10 modules are authorized to use the FCC United States Grants and ISED Canada Certificates of the modules for their own final host products if, as per FCC KDB 996369, the antenna trace design implemented on the host PCB is electrically equivalent to the antenna trace design implemented on the u-blox host PCB used for regulatory type approvals of the modules, described in this section.

☞ In case of antenna trace design change, an FCC Class II Permissive Change and/or ISED Class IV Permissive Change application is required to be filed by the grantee, or the host manufacturer can take responsibility through the change in FCC ID and/or the ISED Multiple Listing (new application) procedure followed by an FCC C2PC and/or ISED C4PC application.

The antenna trace design is implemented on the u-blox host PCB as illustrated in Figure 39, using the parts listed in Table 21, with the support of the additional optional antenna detection capability.

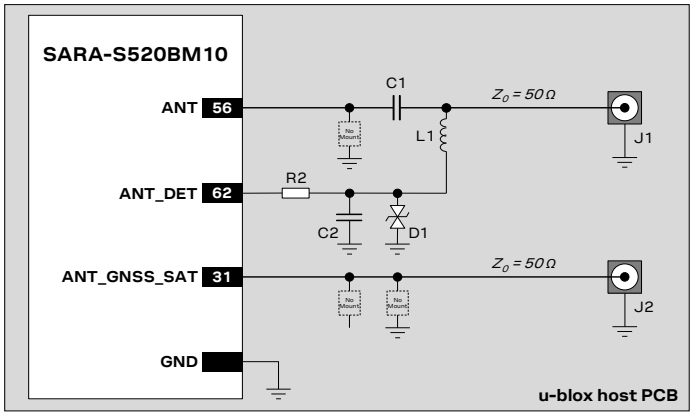

Figure 39: Antenna trace design implemented on the u-blox host PCB, with additional antenna detection circuit

Reference	Description	Part number – Manufacturer
C1	47 pF capacitor ceramic C0G 0201 2% 50 V	GRM0335C1H470GA01 – Murata
C2	39 pF capacitor ceramic C0G 0201 5% 50 V	GRM0332C1H390JA01 – Murata
D1	Low capacitance ESD protection	CG0402MLE-18G – Bourns
L1	82 nH multilayer inductor 0402 (SRF ~1 GHz)	LQG15HS82NJ02B – Murata
R2	10 kΩ resistor 0402 1% 0.063 W	Generic manufacturer
J1, J2	SMA connector 50 Ω through hole jack	SMA6251A1-3GT50G-50 – Amphenol

Table 21: Parts in use on the u-blox host PCB for the antenna trace design, with additional antenna detection circuit

The u-blox host printed circuit board has a structure of 6 copper layers with 35 µm thickness (1 oz/ft^2) for all the layers exect the two inner buried layers, having 18 µm thickness (1/2 oz/ft^2), using FR4 dielectric substrate material with 4.3 typical permittivity and 0.013 typical loss tangent at 1 GHz.

The top layer layout of the u-blox host PCB is described in Figure 40 and Figure 41, implementing the RF antenna trace designed as a 50 Ω grounded coplanar waveguide, with ~23 mm length from the **ANT** pad of the module up to a 50 Ω SMA connector for external LTE cellular antenna and/or RF cable access (Figure 40), and from the **ANT_GNSS_SAT** pad of the module up to a 50 Ω SMA connector for external Satellite antenna and/or RF cable access (Figure 41).

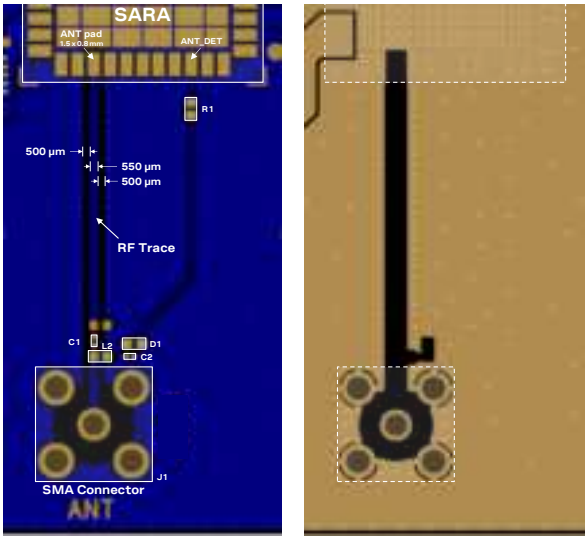

Figure 40: Top layer (L1) and buried layer (L2) layout of the u-blox host PCB with the Cellular antenna RF trace design

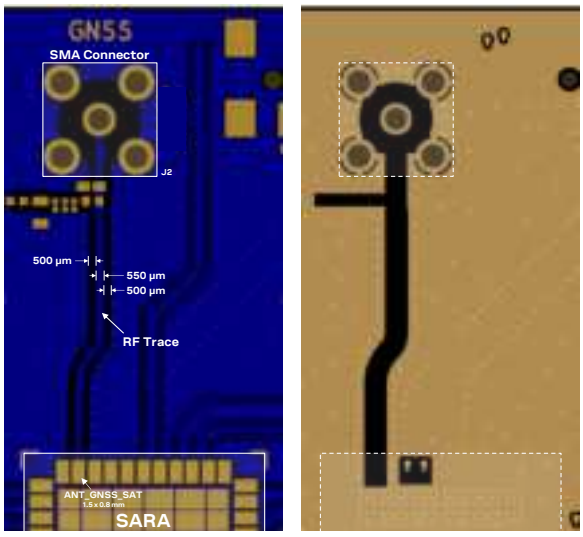

Figure 41: Top layer (L1) and buried layer (L2) layout of the u-blox host PCB with the GNSS / Satellite antenna RF trace design

The PCB stack-up structure of the 6-layer u-blox host printed circuit board is illustrated in Figure 42.

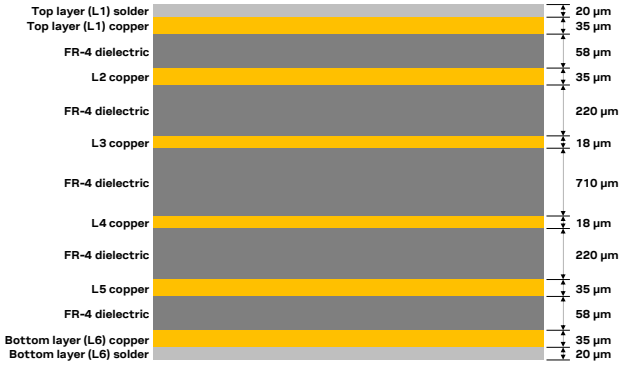

Figure 42: Stack-up structure of the u-blox host PCB

Considering that the thickness of the dielectric material from the top layer to the buried layer is less than 200 µm, GND keep-out is implemented on the buried metal layer area below the **ANT** and/or the **ANT_GNSS_SAT** pad and the antenna RF trace as illustrated in Figure 40 and Figure 41.

Guidelines to design an equivalent proper connection for the **ANT** pad are available in section 2.4.1.1. Guidelines to design an equivalent proper 50 Ω transmission line are available in section 2.4.1.2. Guidelines to design a proper equivalent 50 Ω termination are available in section 2.4.1.3, with further guidelines for cellular antenna selection and design available in section 2.4.2.1. Guidelines to design a proper equivalent (optional) antenna detection circuit are available in section 2.4.5.

The 50 Ω characteristic impedance of the antenna trace design on a host printed circuit board can be verified using a Vector Network Analyzer, as done on the u-blox host PCB, with calibrated RF coaxial cable soldered at the pad corresponding to RF input/output of the module and with the transmission line terminated to a 50 Ω load at the 50 Ω SMA connector.

Compliance of the design with regulatory rules and specifications defined by the FCC, ISED, RED, etc. can be verified using a radio communication tester (callbox) as the Rohde & Schwarz CMW500, or any equivalent equipment for multi-technology signaling conformance tests.

2.5 SIM interface

2.5.1 Guidelines for SIM circuit design

2.5.1.1 Guidelines for SIM cards, SIM connectors and SIM chips selection

The ISO/IEC 7816, the ETSI TS 102 221 and the ETSI TS 102 671 specifications define the physical, electrical and functional characteristics of Universal Integrated Circuit Cards (UICC), which contains the Subscriber Identification Module (SIM) integrated circuit that securely stores all the information needed to identify and authenticate subscribers over the LTE network.

Removable UICC / SIM card contacts mapping is defined by ISO/IEC 7816 and ETSI TS 102 221 as follows:

- Contact C1 = VCC (Supply) → It must be connected to **VSIM**
- Contact C2 = RST (Reset) → It must be connected to **SIM_RST**
- Contact C3 = CLK (Clock) → It must be connected to **SIM_CLK**
- Contact C4 = AUX1 (Auxiliary contact) → It must be left not connected
- Contact C5 = GND (Ground) → It must be connected to **GND**
- Contact C6 = VPP/SWP (Other function) → It can be left not connected
- Contact C7 = I/O (Data input/output) → It must be connected to **SIM_IO**
- Contact C8 = AUX2 (Auxiliary contact) → It must be left not connected

A removable SIM card can have 6 contacts (C1, C2, C3, C5, C6, C7) or 8 contacts, also including the auxiliary contacts C4 and C8. Only 5 contacts are required and must be connected to the module SIM interface.

Removable SIM cards are suitable for applications requiring a change of SIM card during the product lifetime.

A SIM card holder can have 6 or 8 positions if a mechanical card presence detector is not provided, or it can have 6+2 or 8+2 positions if two additional pins relative to the normally-open mechanical switch integrated in the SIM connector for the mechanical card presence detection are provided. Select a SIM connector providing 6+2 or 8+2 positions if the optional SIM detection feature is required by the custom application, otherwise a connector without integrated mechanical presence switch can be selected.

Surface-Mounted UICC / SIM chip contact mapping (M2M UICC Form Factor) is defined by the ETSI TS 102 671 as:

- Case pin 8 = UICC contact C1 = VCC (Supply) → It must be connected to **VSIM**
- Case pin 7 = UICC contact C2 = RST (Reset) → It must be connected to **SIM_RST**
- Case pin 6 = UICC contact C3 = CLK (Clock) → It must be connected to **SIM_CLK**
- Case pin 5 = UICC contact C4 = AUX1 (Aux. contact) → It must be left not connected
- Case pin 1 = UICC contact C5 = GND (Ground) → It must be connected to **GND**
- Case pin 2 = UICC contact C6 = VPP/SWP (Other) → It can be left not connected
- Case pin 3 = UICC contact C7 = I/O (Data I/O) → It must be connected to **SIM_IO**
- Case pin 4 = UICC contact C8 = AUX2 (Aux. contact) → It must be left not connected

A Surface-Mounted SIM chip has 8 contacts and can also include the auxiliary contacts C4 and C8 for other uses, but only 5 contacts are required and must be connected to the module SIM card interface as described above.

Surface-Mounted SIM chips are suitable for M2M applications where it is not required to change the SIM once installed.

2.5.1.2 Guidelines for single SIM card connection without detection

A removable SIM card placed in a SIM card holder must be connected to the SIM card interface of SARA-S520BM10 modules as described in Figure 43, where the optional SIM detection feature is not implemented.

Follow these guidelines to connect the module to a SIM connector without SIM presence detection:

- Connect the UICC / SIM contact C1 (VCC) to the **VSIM** pin of the module.
- Connect the UICC / SIM contact C7 (I/O) to the **SIM_IO** pin of the module.
- Connect the UICC / SIM contact C3 (CLK) to the **SIM_CLK** pin of the module.
- Connect the UICC / SIM contact C2 (RST) to the **SIM_RST** pin of the module.
- Connect the UICC / SIM contact C5 (GND) to ground.
- Provide a 100 nF bypass capacitor (e.g. Murata GRM155R71C104K) on SIM supply line, close to the relative pad of the SIM connector, to prevent digital noise.
- Provide a bypass capacitor of about 22 pF to 47 pF (e.g. Murata GCM1555C1H470JA16) on each SIM line, very close to each related pad of the SIM connector, to prevent RF coupling especially in case the RF antenna is placed closer than 10 – 30 cm from the SIM card holder.
- Provide a very low capacitance (i.e. less than 10 pF) ESD protection (e.g. Tyco PESD0402-140) on each externally accessible SIM line, close to each relative pad of the SIM connector. ESD sensitivity rating of the SIM interface pins is 1 kV (HBM). So that, according to EMC/ESD requirements of the custom application, higher protection level can be required if the lines are externally accessible on the application device.
- Limit capacitance and series resistance on each SIM signal to match the requirements for the SIM interface regarding maximum allowed rise time on the lines.

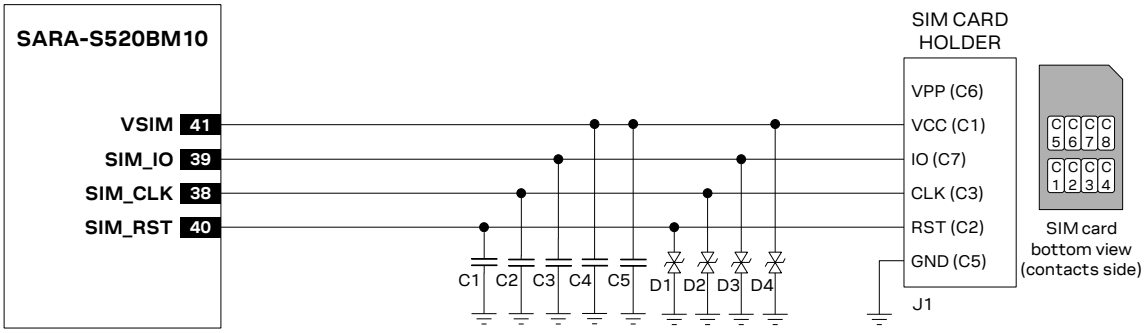

Figure 43: Application circuit for the connection to a single removable SIM card, with SIM detection not implemented

Reference	Description	Part number – Manufacturer
C1, C2, C3, C4	47 pF capacitor ceramic C0G 0402 5% 50 V	GCM1555C1H470JA16 – Murata
C5	100 nF capacitor ceramic X7R 0402 10% 16 V	GCM155R71C104KA55 – Murata
D1, D2, D3, D4	Very low capacitance ESD protection	PESD0402-140 – Tyco Electronics
J1	SIM card holder, 6 positions, without card presence switch	Generic manufacturer, as C707 10M006 136 2 – Amphenol

Table 22: Example of components for the connection to a single removable SIM card, with SIM detection not implemented

2.5.1.3 Guidelines for single SIM chip connection

A Surface-Mounted SIM chip (M2M UICC form factor) must be connected to the SIM card interface of the SARA-S520BM10 modules as described in Figure 44.

Follow these guidelines to connect the module to a Surface-Mounted SIM chip without SIM presence detection:

- Connect the UICC / SIM contact C1 (VCC) to the **VSIM** pin of the module.
- Connect the UICC / SIM contact C7 (I/O) to the **SIM_IO** pin of the module.
- Connect the UICC / SIM contact C3 (CLK) to the **SIM_CLK** pin of the module.
- Connect the UICC / SIM contact C2 (RST) to the **SIM_RST** pin of the module.
- Connect the UICC / SIM contact C5 (GND) to ground.
- Provide a 100 nF bypass capacitor (e.g. Murata GRM155R71C104K) at the SIM supply line close to the relative pad of the SIM chip, to prevent digital noise.
- Provide a bypass capacitor of about 22 pF to 47 pF (e.g. Murata GCM1555C1H470JA16) on each SIM line, to prevent RF coupling especially in case the RF antenna is placed closer than 10 – 30 cm from the SIM lines.
- Limit capacitance and series resistance on each SIM signal to match the requirements for the SIM interface regarding maximum allowed rise time on the lines.

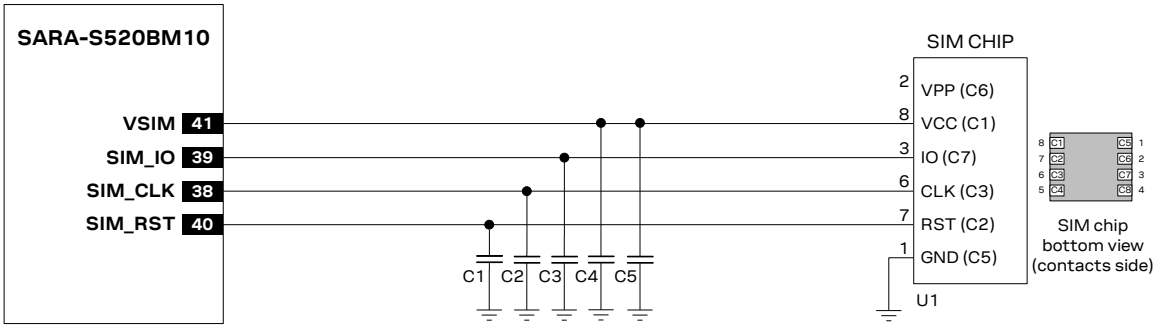

Figure 44: Application circuits for the connection to a single Surface-Mounted SIM chip

Reference	Description	Part number – Manufacturer
C1, C2, C3, C4	47 pF capacitor ceramic C0G 0402 5% 50 V	GCM1555C1H470JA16 – Murata
C5	100 nF capacitor ceramic X7R 0402 10% 16 V	GCM155R71C104KA55 – Murata
U1	SIM chip (M2M UICC form factor)	Generic manufacturer

Table 23: Example of components for the connection to a single SMD SIM chip

2.5.1.4 Guidelines for single SIM card connection with detection

An application circuit for the connection to a single removable SIM card placed in a SIM card holder is described in Figure 45, where the optional SIM card detection feature is implemented.

Follow these guidelines connecting the module to a SIM connector implementing SIM presence detection:

- Connect the UICC / SIM contact C1 (VCC) to the **VSIM** pin of the module.
- Connect the UICC / SIM contact C7 (I/O) to the **SIM_IO** pin of the module.
- Connect the UICC / SIM contact C3 (CLK) to the **SIM_CLK** pin of the module.
- Connect the UICC / SIM contact C2 (RST) to the **SIM_RST** pin of the module.
- Connect the UICC / SIM contact C5 (GND) to ground.

- Connect one pin of the normally-open mechanical switch integrated in the SIM connector (as the SW2 pin in Figure 45) to the **GPIO5** input pin, providing a weak pull-down resistor (e.g. 470 kΩ, as R2 in Figure 45).
- Connect the other pin of the normally-open mechanical switch integrated in the SIM connector (SW1 pin in Figure 45) to **V_INT** 1.8 V supply output by a strong pull-up resistor (e.g. 1 kΩ, as R1 in Figure 45)
- Provide a 100 nF bypass capacitor (e.g. Murata GRM155R71C104K) at the SIM supply line (**VSIM**), close to the related pad of the SIM connector, to prevent digital noise.
- Provide a bypass capacitor of about 22 pF to 47 pF (e.g. Murata GCM1555C1H470JA16) on each SIM line (**VSIM**, **SIM_CLK**, **SIM_IO**, **SIM_RST**), very close to each related pad of the SIM connector, to prevent RF coupling especially in case the RF antenna is placed closer than 10 – 30 cm from the SIM card holder.
- Provide a low capacitance (i.e. less than 10 pF) ESD protection (e.g. Tyco Electronics PESD0402-140) on each externally accessible SIM line, close to each related pad of the SIM connector. The ESD sensitivity rating of SIM interface pins is 1 kV (HBM according to JESD22-A114), so that, according to the EMC/ESD requirements of the custom application, higher protection level can be required if the lines are externally accessible.
- Limit capacitance and series resistance on each SIM signal to match the requirements for the SIM interface regarding maximum allowed rise time on the lines.

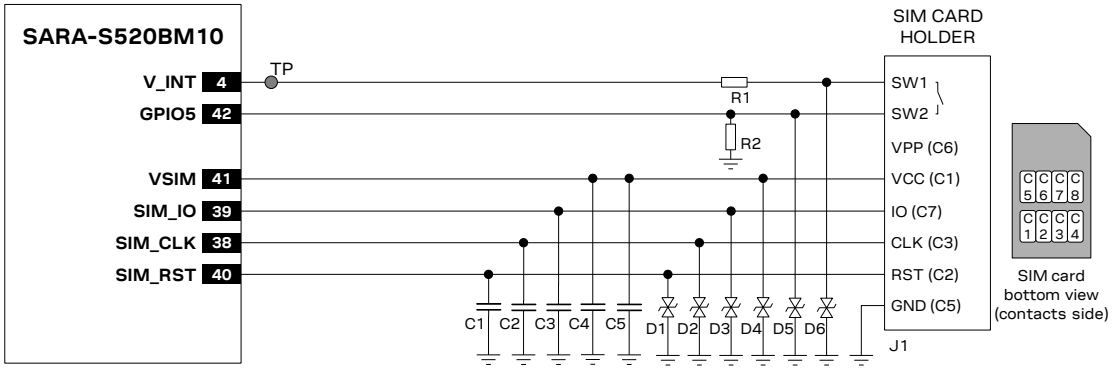

Figure 45: Application circuit for the connection to a single removable SIM card, with SIM detection implemented

Reference	Description	Part number – Manufacturer
C1, C2, C3, C4	47 pF capacitor ceramic C0G 0402 5% 50 V	GCM1555C1H470JA16 – Murata
C5	100 nF capacitor ceramic X7R 0402 10% 16 V	GCM155R71C104KA55 – Murata
D1 – D6	Very low capacitance ESD protection	PESD0402-140 – Tyco Electronics
R1	1 kΩ resistor 0402 5% 0.1 W	Generic manufacturer
R2	470 kΩ resistor 0402 5% 0.1 W	Generic manufacturer
J1	SIM card holder, 6 + 2 positions, with card presence switch	Generic manufacturer, as CCM03-3013LFT R102 – C&K Components

Table 24: Example of components for the connection to a single removable SIM card, with SIM detection implemented

2.5.2 Guidelines for SIM layout design

The layout of the SIM card interface lines (**VSIM**, **SIM_CLK**, **SIM_IO**, **SIM_RST**) may be critical if the SIM card is placed far away from the SARA-S520BM10 modules or in close proximity to the cellular antenna, GNSS antenna or Satellite antenna: these cases should be avoided or at least mitigated as described below.

In the first case, the long connection can cause the radiation of some harmonics of the digital data frequency as any other digital interface. It is recommended to keep the traces short and avoid coupling with RF lines or sensitive analog inputs.

In the second case, the same harmonics can be picked up and create self-interference that can reduce the sensitivity of LTE receiver channels and/or GNSS channels whose carrier frequency is coincidental with harmonic frequencies. It is strongly recommended to place the RF bypass capacitors suggested in Figure 43, Figure 44, and Figure 45 near the SIM connector.

In addition, since the SIM card is typically accessed by the end user, it can be subjected to ESD discharges. Add adequate ESD protection as suggested to protect module SIM pins near the SIM connector.

Limit capacitance and series resistance on each SIM signal to match the SIM specifications. The connections should always be kept as short as possible.

Avoid coupling with any sensitive analog circuit, since the SIM signals can cause the radiation of some harmonics of the digital data frequency.

2.6 Data communication interfaces

2.6.1 UART interfaces

2.6.1.1 Guidelines for UART circuit design

Providing 1 UART with the full RS-232 functionality (using the complete V.24 link)

☞ Compatible with USIO variant 1; not compatible with USIO variants 0/2/3/4 (see section 1.9.1.1).

If RS-232 compatible signal levels are needed, two different external voltage translators (e.g. Maxim MAX3237E and Texas Instruments SN74AVC4T774) can be used. The Texas Instruments chips provide the translation from 1.8 V to 3.3 V, while the Maxim chip provides the translation from 3.3 V to RS-232 compatible signal level.

If a 1.8 V application processor (DTE) is used and complete RS-232 functionality is required, then the complete 1.8 V UART of the module (DCE) should be connected to a 1.8 V DTE, as in Figure 46.

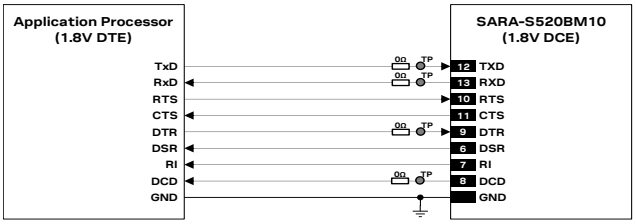

Figure 46: 1 UART interface application circuit with complete V.24 link in DTE/DCE serial communication (1.8 V DTE)

If a 3.0 V application processor (DTE) is used, then it is recommended to connect the 1.8 V UART of the module (DCE) by appropriate unidirectional voltage translators using the module **V_INT** output as 1.8 V supply for the voltage translators on the module side, as described in Figure 47.

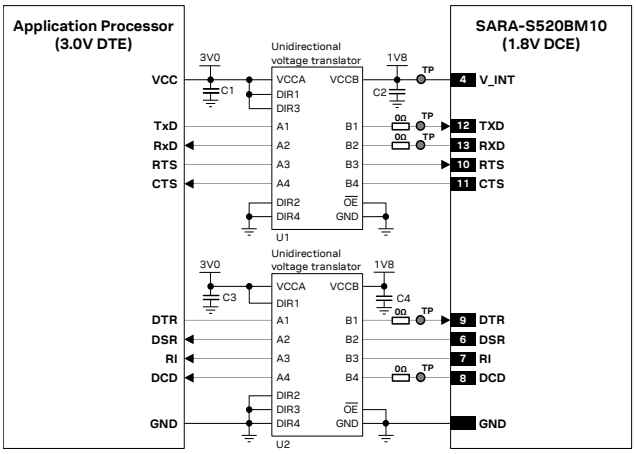

Figure 47: 1 UART interface application circuit with complete V.24 link in DTE/DCE serial communication (3.0 V DTE)

Reference	Description	Part number – Manufacturer
C1, C2, C3, C4	100 nF capacitor ceramic X7R 0402 10% 16 V	GCM155R71C104KA55 – Murata
U1, U2	Unidirectional voltage translator	SN74AVC4T774 [1] - Texas Instruments

Table 25: Components for 1 UART application circuit with complete V.24 link in DTE/DCE serial communication (3.0 V DTE)

☞ Provide accessible test points directly connected to **TXD** and **RXD** pins for FW update purposes; accessible test points may be provided to **DCD** and **DTR** pins for diagnostic purposes, alternatively to the highly recommended test points on the USB interface pins.

[1] Voltage translator providing partial power down feature, so the 3 V supply can be also ramped up before **V_INT** 1.8 V supply

Providing 1 UART with the TXD, RXD, RTS, CTS, DTR and RI lines only

☞ Compatible with USIO variants 0/1; not compatible with USIO variants 2/3/4 (see section 1.9.1.1).

If the functionalities of the **DSR** and **DCD** lines are not required, or the lines are not available:

- Leave **DSR** and **DCD** lines of the module unconnected and floating

If RS-232 compatible signal levels are needed, two different external voltage translators (e.g. Maxim MAX3237E and Texas Instruments SN74AVC4T774) can be used. The Texas Instruments chips provide the translation from 1.8 V to 3.3 V, while the Maxim chip provides the translation from 3.3 V to RS-232 compatible signal level.

Figure 48 describes the circuit that should be implemented if a 1.8 V application processor (DTE) is used, given that the DTE will behave correctly regardless of the **DSR** input setting.

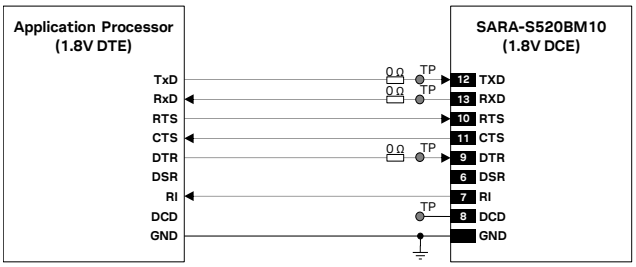

Figure 48: 1 UART interface application circuit with 7-wire link in DTE/DCE serial communication (1.8 V DTE)

If a 3.0 V application processor (DTE) is used, then it is recommended to connect the 1.8 V UART interface of the module (DCE) by appropriate unidirectional voltage translators using the module **V_INT** output as 1.8 V supply for the voltage translators on the module side, as shown in Figure 49, given that the DTE will behave correctly regardless of the **DSR** input setting.

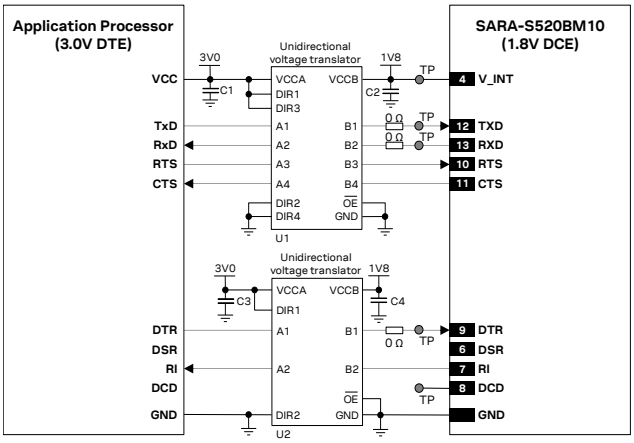

Figure 49: 1 UART interface application circuit with 7-wire link in DTE/DCE serial communication (3.0 V DTE)

Reference	Description	Part number – Manufacturer
C1, C2, C3, C4	100 nF capacitor ceramic X7R 0402 10% 16 V	GCM155R71C104KA55 – Murata
U1	Unidirectional voltage translator	SN74AVC4T774 [2] - Texas Instruments
U2	Unidirectional voltage translator	SN74AVC2T245 [2] – Texas Instruments

Table 26: Components for 1 UART application circuit with 7-wire link in DTE/DCE serial communication (3.0 V DTE)

☞ Provide accessible test points directly connected to **TXD** and **RXD** pins for FW update purposes; accessible test points may be provided to **DCD** and **DTR** pins for diagnostic purposes, alternatively to the highly recommended test points on the USB interface pins.

[2] Voltage translator providing partial power down feature, so the 3 V supply can be also ramped up before **V_INT** 1.8 V supply

Providing 1 UART with the TXD, RXD, RTS and CTS lines only

☞ Compatible with USIO variants 0/1/3; not compatible with USIO variants 2/4 (see section 1.9.1.1).

If the functionalities of the **DSR**, **DCD**, **RI** and **DTR** lines are not required, or the lines are not available:

- Connect the **DTR** input to GND, as useful to have the greeting text presented over the UART,
- Leave **DSR**, **DCD**, and **RI** lines of the module floating

If RS-232 compatible signal levels are needed, the Maxim MAX13234E voltage level translator can be used. This chip translates voltage levels from 1.8 V (module side) to the RS-232 standard.

If a 1.8 V application processor is used, the circuit should be implemented as described in Figure 50.

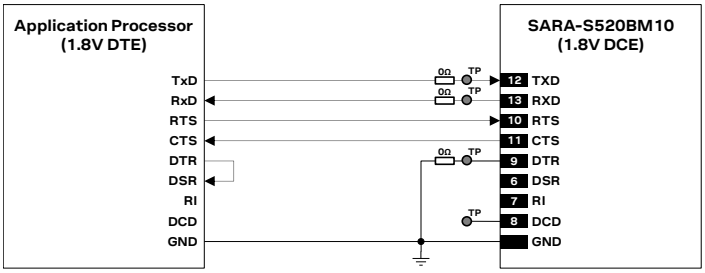

Figure 50: 1 UART interface application circuit with 5-wire link in DTE/DCE serial communication (1.8V DTE)

If a 3.0 V application processor (DTE) is used, then it is recommended to connect the 1.8 V UART interface of the module (DCE) by an appropriate unidirectional voltage translator using the module **V_INT** output as 1.8 V supply for the voltage translator on the module side, as in Figure 51.

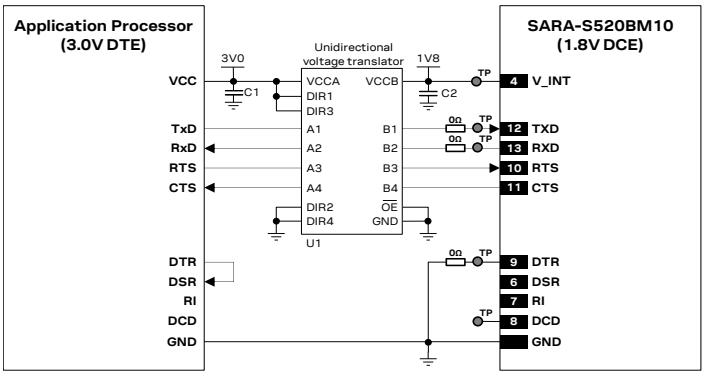

Figure 51: 1 UART interface application circuit with 5-wire link in DTE/DCE serial communication (3.0 V DTE)

Reference	Description	Part number – Manufacturer
C1, C2	100 nF capacitor ceramic X7R 0402 10% 16 V	GCM155R71C104KA55 – Murata
U1	Unidirectional voltage translator	SN74AVC4T774 [3] - Texas Instruments

Table 27: Components for 1 UART application circuit with 5-wire link in DTE/DCE serial communication (3.0 V DTE)

☞ Provide accessible test points directly connected to **TXD** and **RXD** pins for FW update purposes; accessible test points may be provided to **DCD** and **DTR** pins for diagnostic purposes, alternatively to the highly recommended test points on the USB interface pins.

[3] Voltage translator providing partial power down feature, so the 3 V supply can be also ramped up before **V_INT** 1.8 V supply

Providing 2 UARTs with the TXD, RXD, RTS and CTS lines only

☞ Compatible with USIO variants 2/3/4; not compatible with USIO variants 0/1 (see section 1.9.1.1).

If RS-232 compatible signal levels are needed, two Maxim MAX13234E voltage level translators can be used. These chips translate voltage levels from 1.8 V (module side) to the RS-232 standard.

If a 1.8 V application processor is used, the circuit should be implemented as described in Figure 52.

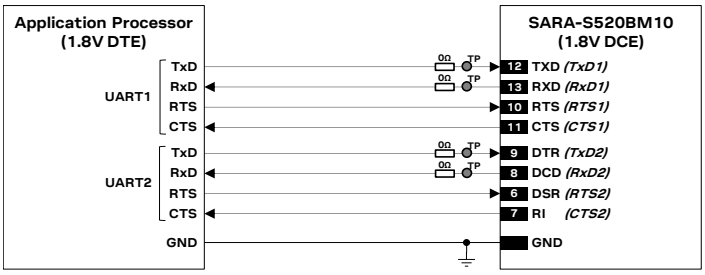

Figure 52: 2 UART interfaces application circuit with 5-wire links in DTE/DCE serial communications (1.8 V DTE)

If a 3.0 V application processor (DTE) is used, then it is recommended to connect the 1.8 V UART interfaces of the module (DCE) by appropriate unidirectional voltage translators using the module **V_INT** output as 1.8 V supply for the voltage translators on the module side, as in Figure 53.

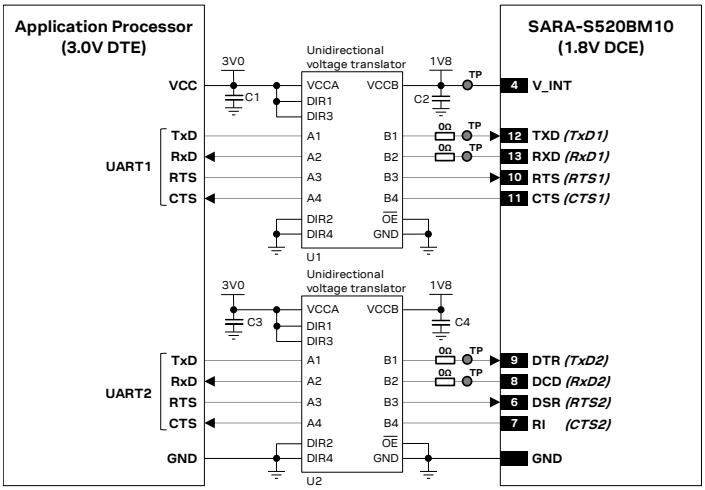

Figure 53: 2 UART interfaces application circuit with 5-wire links in DTE/DCE serial communications (3.0 V DTE)

Reference	Description	Part number – Manufacturer
C1, C2, C3, C4	100 nF capacitor ceramic X7R 0402 10% 16 V	GCM155R71C104KA55 – Murata
U1, U2	Unidirectional voltage translator	SN74AVC4T774 [4] - Texas Instruments

Table 28: Components for 2 UARTs application circuit with 5-wire links in DTE/DCE serial communications (3.0 V DTE)

☞ Provide accessible test points directly connected to **TXD** and **RXD** pins for FW update purposes; accessible test points may be provided to **DCD** and **DTR** pins for diagnostic purposes, alternatively to the highly recommended test points on the USB interface pins.

[4] Voltage translator providing partial power down feature, so the 3 V supply can be also ramped up before **V_INT** 1.8 V supply

Providing 1 UART with the TXD and RXD lines only

☞ Compatible with USIO variants 0/1/3; not compatible with USIO variants 2/4 (see section 1.9.1.1).

☞ Providing the **TXD** and **RXD** lines only is not recommended if the multiplexer functionality is used in the application: providing also at least the HW flow control (**RTS** and **CTS** lines) is recommended, and it is particularly necessary if the low power mode is enabled by +UPSV AT command.

If the functionalities of the **RTS**, **CTS**, **DTR**, **DSR**, **RI** and **DCD** lines are not required in the application, or the lines are not available, then:

- Connect the module **RTS** input to GND or to the module **CTS** output, since the module requires **RTS** active (low electrical level) if HW flow control is enabled (as it is by default),
- Connect the **DTR** input to GND, as useful to have the greeting text presented over the UART,
- Leave **DSR**, **RI** and **DCD** lines of the module floating

If RS-232 compatible signal levels are needed, the Maxim MAX13236E voltage level translator can be used. This chip translates voltage levels from 1.8 V (module side) to the RS-232 standard.

If a 1.8 V application processor (DTE) is used, the circuit should be implemented as in Figure 54.

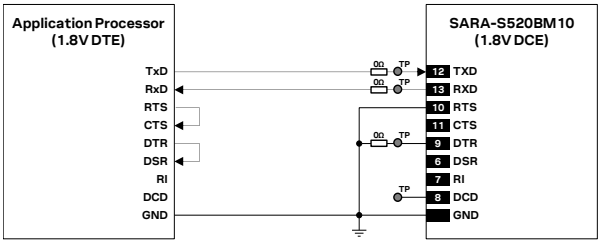

Figure 54: 1 UART interface application circuit with 3-wire link in DTE/DCE serial communication (1.8 V DTE)

If a 3.0 V application processor (DTE) is used, then it is recommended to connect the 1.8 V UART interface of the module (DCE) by an appropriate unidirectional voltage translator using the module **V_INT** output as 1.8 V supply for the voltage translator on the module side, as in Figure 55.

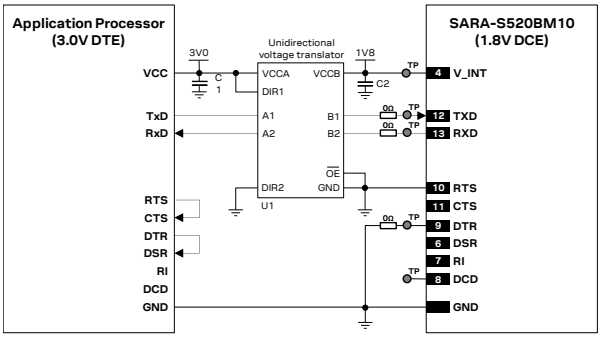

Figure 55: 1 UART interface application circuit with 3-wire link in DTE/DCE serial communication (3.0 V DTE)

Reference	Description	Part number – Manufacturer
C1, C2	100 nF capacitor ceramic X7R 0402 10% 16 V	GCM155R71C104KA55 – Murata
U1	Unidirectional voltage translator	SN74AVC2T245 [5] - Texas Instruments

Table 29: Components for 1 UART application circuit with 3-wire link in DTE/DCE serial communication (3.0 V DTE)

☞ Provide accessible test points directly connected to **TXD** and **RXD** pins for FW update purposes; accessible test points may be provided to **DCD** and **DTR** pins for diagnostic purposes, alternatively to the highly recommended test points on the USB interface pins.

[5] Voltage translator providing partial power down feature, so the 3 V supply can be also ramped up before **V_INT** 1.8 V supply

Providing 2 UARTs with the TXD and RXD lines only

Compatible with USIO variants 2/3/4; not compatible with USIO variants 0/1 (see section 1.9.1.1).

Providing the **TXD** and **RXD** lines only is not recommended if the multiplexer functionality is used in the application: providing also at least the HW flow control (**RTS** and **CTS** lines) is recommended, and it is in particular necessary if the low power mode is enabled by +UPSV AT command.

If the functionalities of the **RTS**, **CTS**, **DSR** and **RI** lines are not required in the application, or the lines are not available, then:

- Connect the module **RTS** and **DSR** input lines to GND or respectively to the **CTS** and **RI** output of the module, since the module requires **RTS** and **DSR** active (low electrical level) if HW flow control is enabled (as it is by default)

If RS-232 compatible signal levels are needed, the Maxim MAX13234E voltage level translator can be used. This chip translates voltage levels from 1.8 V (module side) to the RS-232 standard.

If a 1.8 V application processor (DTE) is used, the circuit should be implemented as in Figure 56.

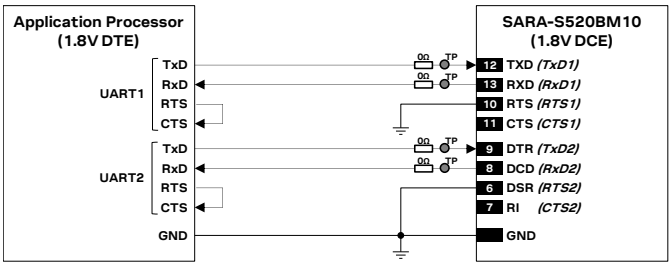

Figure 56: 2 UART interfaces application circuit with 3-wire links in DTE/DCE serial communications (1.8 V DTE)

If a 3.0 V application processor (DTE) is used, then it is recommended to connect the 1.8 V UART interfaces of the module (DCE) by an appropriate unidirectional voltage translator using the module **V_INT** output as 1.8 V supply for the voltage translator on the module side, as in Figure 55.

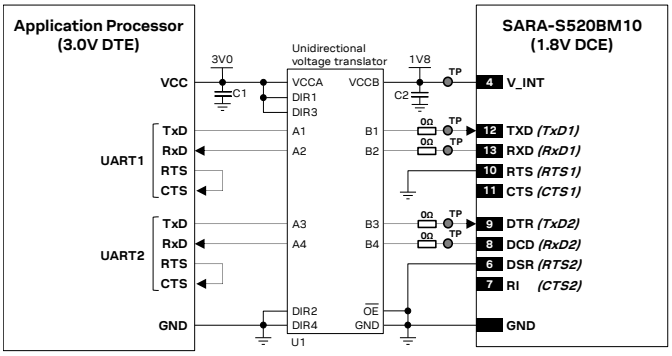

Figure 57: 2 UART interfaces application circuit with 3-wire links in DTE/DCE serial communications (3.0 V DTE)

Reference	Description	Part number – Manufacturer
C1, C2	100 nF capacitor ceramic X7R 0402 10% 16 V	GCM155R71C104KA55 – Murata
U1	Unidirectional voltage translator	SN74AVC4T774 [6] - Texas Instruments

Table 30: Components for 2 UARTs application circuit with 3-wire links in DTE/DCE serial communications (3.0 V DTE)

Provide accessible test points directly connected to **TXD** and **RXD** pins for FW update purposes; accessible test points may be provided to **DCD** and **DTR** pins for diagnostic purposes, alternatively to the highly recommended test points on the USB interface pins.

[6] Voltage translator providing partial power down feature, so the 3 V supply can be also ramped up before **V_INT** 1.8 V supply

Additional considerations

If a 3.0 V application processor (DTE) is used, the voltage scaling from any 3.0 V output of the DTE to the corresponding 1.8 V input of the module (DCE) can be implemented, as an alternative low-cost solution, by an appropriate voltage divider. Consider the value of the pull-down / pull-up integrated at the input of the module (DCE) for the correct selection of the voltage divider resistance values. Make sure that any DTE signal connected to the module is tri-stated or set low when the module is in power-down mode and during the module power-on sequence (at least until the activation of the **V_INT** supply output of the module), to avoid latch-up of circuits and allow a clean boot of the module (see the remark below).

Moreover, the voltage scaling from any 1.8 V output of the cellular module (DCE) to the corresponding 3.0 V input of the application processor (DTE) can be implemented by an appropriate low-cost non-inverting buffer with open drain output. The non-inverting buffer should be supplied by the **V_INT** supply output of the cellular module. Consider the value of the pull-up integrated at each input of the DTE (if any) and the baud rate required by the application for the appropriate selection of the resistance value for the external pull-up biased by the application processor supply rail.

- It is highly recommended to provide accessible test points directly connected to the **TXD** and **RXD** pins for FW upgrade purposes, in particular providing a 0 Ω series jumper on each line to detach each pin of the module from the DTE application processor; accessible test points may be provided to **DCD** and **DTR** pins for diagnostic purposes, alternatively to the highly recommended test points on the USB interface pins.
- Do not apply voltage to any UART interface pin before the switch-on of the UART supply source (**V_INT**), to avoid latch-up of circuits and allow a clean boot of the module.
- ESD sensitivity rating of the UART interface pins is 1 kV (Human Body Model according to JESD22-A114). Higher protection levels could be required if the lines are externally accessible, and it can be achieved by mounting an ESD protection (e.g., EPCOS CA05P4S14THSG varistor array) close to the accessible points.

2.6.1.2 Guidelines for UART layout design

The UART serial interface requires the same consideration regarding electro-magnetic interference as any other digital interface. Keep the traces short and avoid coupling with RF line or sensitive analog inputs, since the signals can cause the radiation of some harmonics of the digital data frequency.

2.6.2 USB interface

The USB interface is available for diagnostic purposes only.

2.6.2.1 Guidelines for USB circuit design

A suitable application circuit can be similar to the one illustrated in Figure 58, where direct external access is provided for diagnostic purposes by test points made available on the application board for **VUSB_DET**, **USB_D+** and **USB_D-** lines.

USB pull-up or pull-down resistors and external series resistors on **USB_D+** and **USB_D-** lines as required by the USB 2.0 specification [3] are part of the module USB pins driver and do not need to be externally provided.

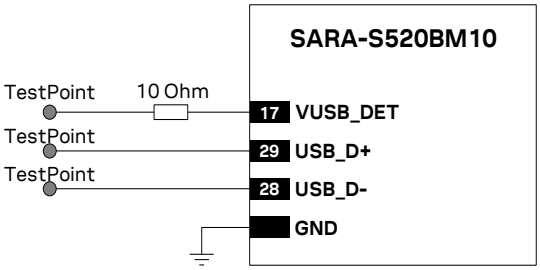

Figure 58: SARA-S520BM10 modules USB application circuit providing access for diagnostic purposes

It is highly recommended to provide accessible test points directly connected to the USB interface pins (**VUSB_DET**, **USB_D+**, **USB_D-**) for diagnostic purposes.

It is recommended to include a 10 Ohm series resistor (0402 or similar) along the **VUSB_DET** input line to avoid exceeding the related absolute maximum rating for the voltage ramp.

The USB interface pins ESD sensitivity rating is 1 kV (HBM according to JESD22-A114F). Higher protection level could be required if the lines are externally accessible and it can be achieved by mounting a very low capacitance (i.e. less or equal to 1 pF) ESD protection (e.g. the Littelfuse PESD0402-140 ESD protection) on the lines connected to these pins, close to accessible points.

2.6.2.2 Guidelines for USB layout design

USB_D+ / **USB_D-** lines should be designed with differential characteristic impedance (Z_0) as close as possible to 90 Ω and with common mode characteristic impedance (Z_{CM}) as close as possible to 30 Ω as defined by the USB 2.0 specification [3], routed as differential pair, with length as short as possible, avoiding any stubs, and avoiding abrupt change of layout.

However, the USB interface is available for diagnostic purposes only, and therefore the layout is not very critical: **USB_D+** / **USB_D-** lines have to be routed as differential pair, with short length, up to the related test points as illustrated in Figure 58.

2.6.3 SPI interface

SPI interface is not supported by SARA-S520BM10 products version, except for diagnostic.

Accessible test points directly connected to the **SDIO_D0**, **SDIO_D1**, **SDIO_D2** and **SDIO_D3** pins may be provided for diagnostic purposes, alternatively to the highly recommended test points on the USB interface pins.

2.6.4 SDIO interface

☞ SDIO interface is not supported by SARA-S520BM10 products version, except for diagnostic.

☞ Accessible test points directly connected to the **SDIO_D0**, **SDIO_D1**, **SDIO_D2** and **SDIO_D3** pins may be provided for diagnostic purposes, alternatively to the highly recommended test points on the USB interface pins.

2.6.5 I2C interface

☞ Communication with an external GNSS receiver is not supported by SARA-S520BM10 modules.

2.6.5.1 Guidelines for I2C circuit design

The I2C-bus host interface can be used to communicate with external I2C-bus devices.

The **SDA** and **SCL** pins of the module are open drain output as per I2C bus specifications [9], and they have internal pull-up resistors to the **V_INT** 1.8 V supply rail of the module, so there is no need of additional pull-up resistors on the external application board.

☞ Capacitance and series resistance must be limited on the bus to match the I2C specifications (1.0 µs is the max allowed rise time on **SCL** and **SDA** lines): route connections as short as possible.

☞ ESD sensitivity rating of the I2C pins is 1 kV (HBM according to JESD22-A114). Higher protection level could be required if the lines are externally accessible and it can be achieved by mounting an ESD protection (e.g. EPCOS CA05P4S14THSG varistor) close to accessible points.

2.6.5.2 Guidelines for I2C layout design

The I2C serial interface requires the same consideration regarding electro-magnetic interference as any other digital interface. Keep the traces short and avoid coupling with RF line or sensitive analog inputs, since the signals can cause the radiation of some harmonics of the digital data frequency.

2.7 ADC

SARA-S520BM10 modules include an analog-to-digital converter input pin, **ADC**, configurable via a dedicated AT command (for further details, see the AT commands manual [2]).

2.7.1 Guidelines for ADC circuit design

As a design example, the **ADC** input pin can be connected to an external voltage divider for voltage measurement purpose as illustrated in Figure 59.

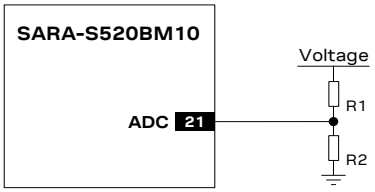

Figure 59: ADC application circuit example

☞ ESD sensitivity rating of the **ADC** pin is 1 kV (Human Body Model according to JESD22-A114). A higher protection level may be required if the lines are externally accessible. This can be achieved by mounting an ESD protection (e.g. EPCOS CA05P4S14THSG varistor) close to accessible points.

2.7.2 Guidelines for ADC layout design

The ADC circuit requires careful layout to perform proper measurements. Make sure that no transient noise is coupled on this line, otherwise the measurements might be affected. It is recommended to keep the connection line to **ADC** as short as possible.

2.8 General purpose input / output (GPIO)

2.8.1 Guidelines for GPIO circuit design

A typical usage of SARA-S520BM10 modules' GPIOs can be the following:

- Network indication provided over **GPIO1** pin (see Figure 60 / Table 31 below)
- Module status / operating mode indication provided by a GPIO pin (see section 1.6.1)
- SIM card detection function provided over **GPIO5** pin (see Figure 45 / Table 24 in section 2.5)
- Time pulse function provided over **GPIO6** pin (see section Figure 60 / Table 31 below)

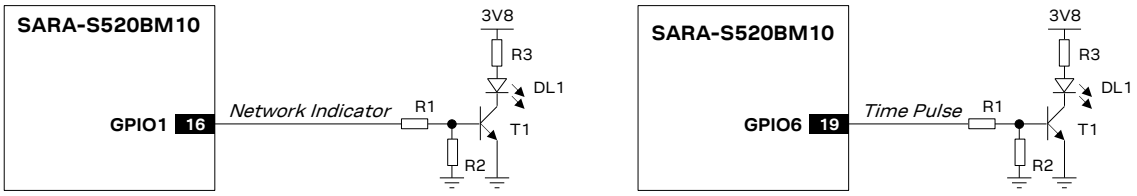

Figure 60: Application circuit for network indication provided over GPIO1 and/or time pulse provided over GPIO6

Reference	Description	Part number – Manufacturer
R1	10 kΩ resistor 0402 5% 0.1 W	Generic manufacturer
R2	47 kΩ resistor 0402 5% 0.1 W	Generic manufacturer
R3	820 Ω resistor 0402 5% 0.1 W	Generic manufacturer
DL1	LED red SMT 0603	LTST-C190KRKT – Lite-on Technology Corporation
T1	NPN BJT transistor	BC847 – Infineon

Table 31: Components for network indication and/or time pulse application circuit

- Use transistors with at least an integrated resistor in the base pin or otherwise put a 10 kΩ resistor on the board in series to the GPIO of SARA-S520BM10 modules.
- Do not apply voltage to any GPIO of the module before the switch-on of the GPIOs supply (**V_INT**), to avoid latch-up of circuits and allow a clean module boot.
- ESD sensitivity rating of the GPIO pins is 1 kV (Human Body Model according to JESD22-A114). Higher protection level could be required if the lines are externally accessible and it can be achieved by mounting an ESD protection (e.g. EPCOS CA05P4S14THSG varistor) close to accessible points.
- If the GPIO pins are not used, they can be left unconnected on the application board.

2.8.2 Guidelines for general purpose input/output layout design

The general purpose input / output pins are generally not critical for layout.

2.9 GNSS peripheral output

2.9.1 Guidelines for GNSS peripheral output circuit design

SARA-S520BM10 modules provide the following 1.8 V peripheral output pins directly connected to the internal u-blox M10 GNSS chipset (as is illustrated in Figure 2):

- The **TXD_GNSS** pin consisting in the UART data output of the internal u-blox GNSS chipset: the line can be connected to a UART data input of the application processor (see Figure 61).

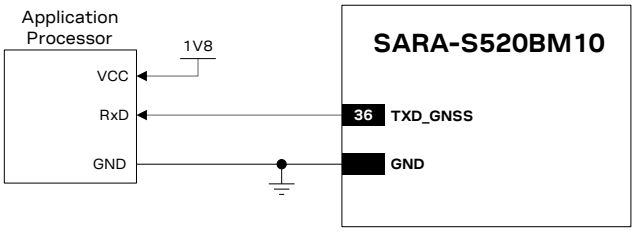

Figure 61: Application circuit for GNSS peripheral UART data output pin

2.9.2 Guidelines for GNSS peripheral output layout design

The GNSS peripheral output pins are generally not critical for layout.

2.10 GNSS real-time clock

2.10.1 Guidelines for GNSS RTC circuit design

The real-time clock (RTC) is a part of the backup domain. The RTC is internally supplied when the GNSS receiver is switched on, or it is optionally supplied through the **V_BCKP_GNSS** pin when GNSS is switched off. The RTC is continuously calibrated when the receiver has GNSS position fix. The RTC is used to maintain time during the backup modes and the on/off operation of the power save mode (PSMOO). Time information is required for hot starts and warm starts.

The GNSS RTC can be fed by providing an external 32.768 kHz clock signal to the **RTC_GNSS** input pin, as described in Figure 62 and Table 32. The external clock signal must always be available to allow the receiver to perform a periodical offset calibration for the RTC clock.

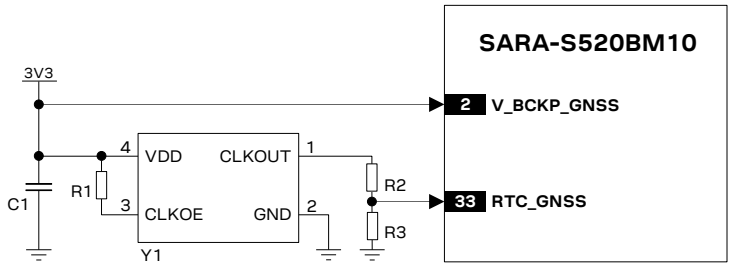

Figure 62: GNSS RTC application circuit with clock provided externally

Reference	Description	Part number – Manufacturer
C1	100 nF capacitor ceramic X7R 0402 10% 16 V	GCM155R71C104KA55 – Murata
R1	100 kΩ resistor 0402 5% 0.1 W	Generic manufacturer
R2	33 kΩ resistor 0402 1% 1/16 W	Generic manufacturer
R3	18 kΩ resistor 0402 1% 1/16 W	Generic manufacturer
Y1	Low power clock oscillator 32.768 kHz	OV-7604-C7 – Micro Crystal

Table 32: Components for GNSS RTC application circuit with clock provided externally

☞ The GNSS RTC signal must be connected without a DC block.

Alternatively, it can be enabled with a dedicated AT command and internally generated as long as the module does not enter deep-sleep mode or does not switch-off; in this case, the **RTC_GNSS** pin must be left unconnected, as described in Figure 63.

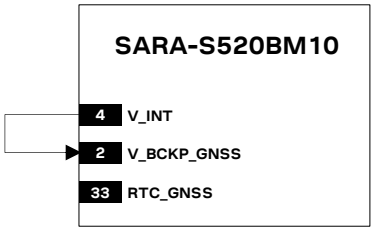

Figure 63: GNSS RTC application circuit with clock generated internally

To enable the GNSS RTC in hardware backup mode, the GNSS backup domain must also be supplied, as shown in Figure 62 and Figure 63 (see section 2.2.3).

Leave **RTC_GNSS** pin unconnected if GNSS RTC is not used.

2.10.2 Guidelines for GNSS RTC layout design

If clock is provided externally, the GNSS RTC circuit (**RTC_GNSS**) requires careful layout; it is recommended to keep the trace short and avoid coupling with RF lines, other digital lines or any sensitive analog circuit.

2.11 Module placement

An optimized placement allows minimum RF lines' length and closer path from DC source for **VCC**.

Make sure that the module, analog parts and RF circuits are clearly separated from any possible source of radiated energy. In particular, digital circuits can radiate digital frequency harmonics, which can produce electro-magnetic interference that affects the module, analog parts and RF circuits' performance. Implement suitable countermeasures to avoid any possible electro-magnetic compatibility issue.

Make sure that the module is placed in order to keep the antennas as far as possible from VCC supply line and related parts (see Figure 23), from high-speed digital lines and from any possible noise source.

Provide enough clearance between the module and any external part: clearance of at least 0.4 mm per side is recommended to let suitable mounting of the parts.

The heat dissipation during RF transmission at roughly 31.5 dBm output power, as required for the connectivity with ORBCOMM Satellite service, can raise the temperature of the application baseboard below the SARA-S520BM10 modules: avoid placing temperature sensitive devices close to the module (see section 2.13 for further thermal guidelines).

2.12 Module footprint and paste mask

Figure 64 and Table 33 describe the suggested footprint (i.e. copper mask) and paste mask layout for SARA modules: the proposed land pattern layout reflects the modules' pins layout, while the proposed stencil apertures layout is slightly different (see the F'', H'', I'', J'', O'' parameters compared to the F', H', I', J', O' ones).

The Non Solder-resist Mask Defined (NSMD) pad type is recommended over the Solder-resist Mask Defined (SMD) pad type, as it implements the solder resist mask opening 50 µm larger per side than the corresponding copper pad.

The recommended thickness of the stencil for the soldering paste is 150 µm, according to application production process requirements.

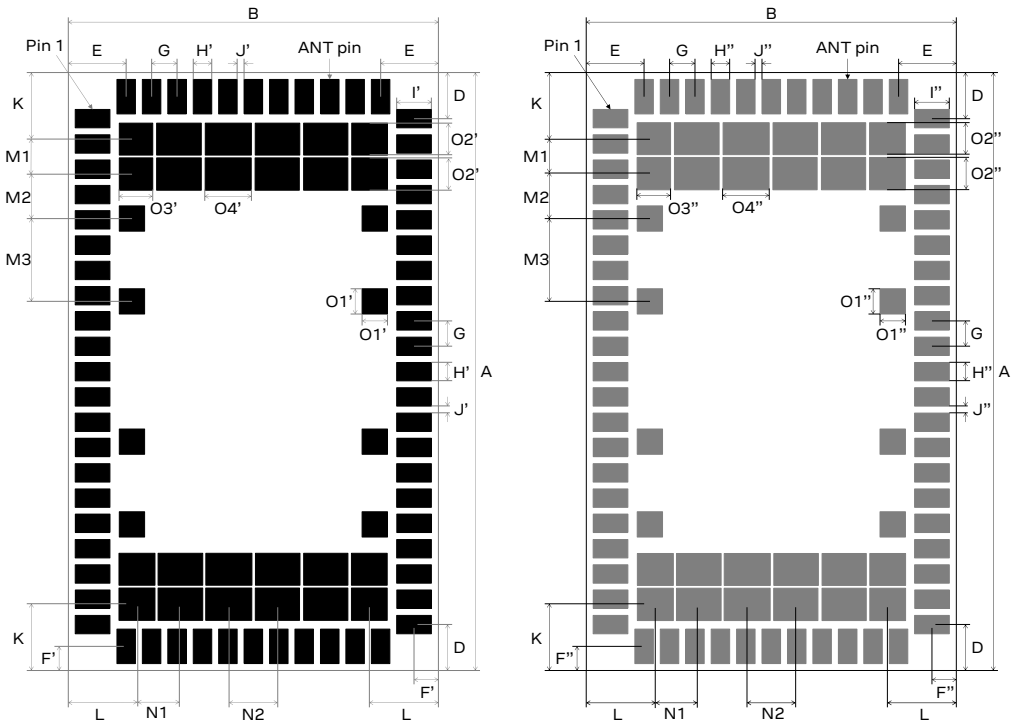

Figure 64: SARA-S520BM10 modules suggested footprint and paste mask (application board top view)

Parameter	Value	Parameter	Value	Parameter	Value
A	26.0 mm	I'	1.50 mm	N2	2.10 mm
B	16.0 mm	I''	1.55 mm	O1'	1.10 mm
C	2.40 mm	J'	0.30 mm	O1''	1.05 mm
D	2.00 mm	J''	0.35 mm	O2'	1.40 mm
E	2.50 mm	K	2.90 mm	O2''	1.35 mm
F'	1.05 mm	L	2.975 mm	O3'	1.55 mm
F''	1.00 mm	M1	1.50 mm	O3''	1.50 mm
G	1.10 mm	M2	1.95 mm	O4'	2.0 mm
H'	0.80 mm	M3	3.60 mm	O4''	1.95 mm
H''	0.75 mm	N1	1.875 mm		

Table 33: SARA-S520BM10 modules suggested footprint and paste mask dimensions

☞ These are recommendations only and not specifications. The exact copper, solder and paste mask geometries, distances, stencil thicknesses and solder paste volumes must be adapted to the specific production processes (e.g. soldering, etc.) implemented.

2.13 Thermal guidelines

☞ The module operating temperature range is specified in the SARA-S520BM10 data sheet [1].

The most critical condition concerning module thermal dissipation is the uplink transmission in Satellite connected mode, as in this case the RF output power is always set at roughly +31.5 dBm, according to ORBCOMM Satellite system specifications (see section 1.5.1.2 for more details).

During Satellite uplink RF transmission, the SARA-S520BM10 modules may generate up to ~10 W thermal power: this is an indicative value since the exact generated power depends on operating conditions, such as the actual antenna return loss, the temperature, the nominal voltage, etc.

The power consumption of the SARA-S520BM10 modules during uplink transmission in terrestrial Cellular LTE mode is less significant in magnitude as compared to the one during Satellite connected mode, as the RF output power can vary depending on Cellular LTE network condition (see the Terminal Tx Power distributiontaken from operation on a live network in the GSMA TS.09 Document [10]), and the maximum RF output power is set at +23 dBm (see section 1.5.1.3 for more details).

☞ For detailed module consumption values, see the SARA-S520BM10 data sheet [1].

The generated thermal power must be adequately dissipated through the thermal and mechanical design of the application.

The increase of the thermal dissipation, i.e. the reduction of the Module-to-Ambient thermal resistance, will decrease the temperature of the module's internal circuitry for a given operating ambient temperature. This improves the device's long-term reliability in particular for applications operating at high ambient temperature.

Instead, the internal 26 MHz Temperature-Controlled Crystal Oscillator (TCXO) needs to be isolated as much as possible from thermal heating.

Recommended hardware techniques to be used to improve heat dissipation in the application:

- Provide an optimal ground connection of the **GND** pins in the area where the internal Satellite Power Amplifier is located (see Figure 24, section 2.2.1.10), increasing as much as possible the number of vias for the GND pins on the application board located in this area down to the application board solid ground layer.
- Provide a weak ground connection of the **GND** pins in the area where the internal TCXO is located (see Figure 24, section 2.2.1.10).
- Connect each ground area of the multilayer application PCB with complete thermal via stacked down to main ground layer.
- Provide a ground plane as wide as possible on the application board.
- Optimize antenna return loss, to optimize overall electrical performance of the module including a decrease of module thermal power.
- Optimize the thermal design of any high-power components included in the application, such as linear regulators and amplifiers, to optimize overall temperature distribution in the application.
- Select the material, the thickness and the surface of the box (i.e. the mechanical enclosure) of the application device that integrates the module so that it provides good thermal dissipation.

Further HW techniques that may be considered to improve the heat dissipation in the application:

- Force ventilation air-flow within the mechanical enclosure.
- Provide a heat sink component attached to the module top side, with electrically insulated / high thermal conductivity adhesive, or on the backside of the application board, below the cellular module, as a large part of the heat is transported through the GND pads of the LGA modules and dissipated over the backside of the application board.

2.14 Schematic for SARA-S520BM10 module integration

Figure 65 is an example schematic diagram where a SARA-S520BM10 module is integrated into an application board using most of the available interfaces and functions of the module.

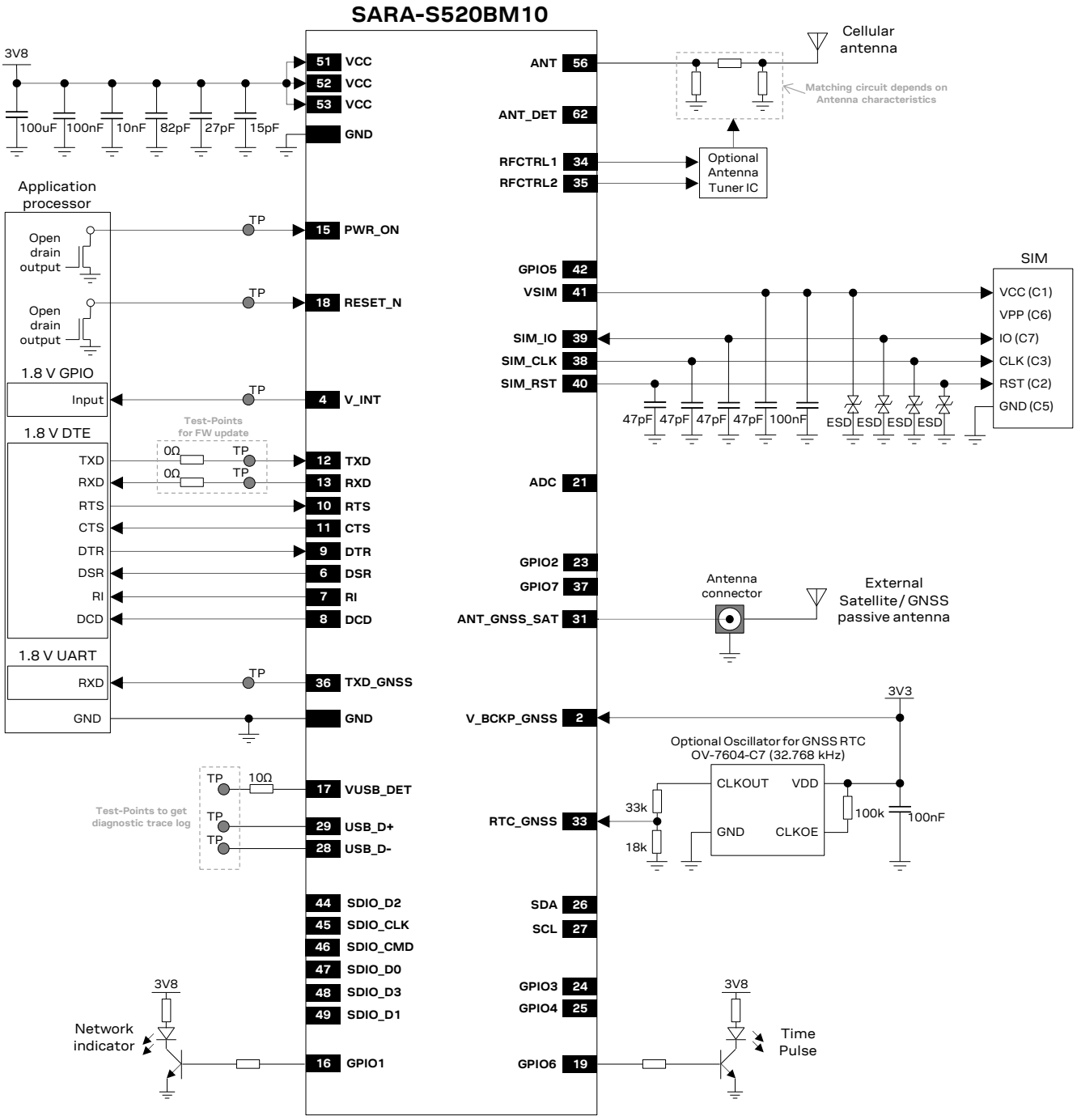

Figure 65: Example schematic diagram integrating a SARA-S520BM10 module

2.15 Design-in checklist

This section provides a design-in checklist.

2.15.1 Schematic checklist

The following are the most important points for a simple schematic check:

- ☑ DC supply must provide a nominal voltage at **VCC** pin within the operating range limits.
- ☑ DC supply must be capable of supporting with adequate safe design margin the highest current consumption values during transmissions to the Satellite system, considering the data shown in SARA-S520BM10 data sheet [1] with normal ambient temperature and voltage conditions.
- ☑ **VCC** voltage supply should be clean, with very low ripple/noise: provide the suggested bypass capacitors, in particular if the application device integrates an internal antenna.
- ☑ Do not apply loads which might exceed the limit for maximum available current from **V_INT** supply.
- ☑ Check that voltage level of any connected pin does not exceed the relative operating range.
- ☑ Provide accessible test points directly connected to the **V_INT**, **PWR_ON** and **RESET_N** pins of the SARA-S520BM10 modules for diagnostic purposes.
- ☑ Capacitance and series resistance must be limited on each SIM signal to match the SIM specifications.
- ☑ Insert the suggested pF capacitors on each SIM signal and low capacitance ESD protections if accessible.
- ☑ Check UART signals direction, considering the modules' signal names follow the ITU-T V.24 recommendation [4].
- ☑ Provide accessible test points directly connected to the **TXD** and **RXD** pins of SARA-S520BM10 modules for FW update purpose, in particular providing a 0 Ω series jumper on each line to detach each pin of the module from the DTE application processor.
- ☑ Provide accessible test points directly connected to the **VUSB_DET**, **USB_D+** and **USB_D-** pins of the SARA-S520BM10 modules for diagnostic purposes.
- ☑ Use transistors with at least an integrated resistor in the base pin or otherwise put a 10 kΩ resistor on the board in series to the GPIO when those are used to drive LEDs.
- ☑ Provide adequate precautions for EMC / ESD immunity as required on the application board.
- ☑ Do not apply voltage to any generic digital interface pin of SARA-S520BM10 modules before the switch-on of the generic digital interface supply source (**V_INT**).
- ☑ All unused pins can be left unconnected.

2.15.2 Layout checklist

The following are the most important points for a simple layout check:

- ☑ Check 50 Ω nominal characteristic impedance of the RF transmission line connected to the **ANT** port (cellular antenna RF interface).
- ☑ Check cellular antenna trace design for regulatory compliance perspective (see section 4.2 for FCC United States, section 4.3 for ISED Canada).
- ☑ Check 50 Ω nominal characteristic impedance of the RF transmission line connected to the **ANT_GNSS_SAT** port (Satellite / GNSS antenna RF interface).
- ☑ Ensure no coupling occurs between the RF interfaces and noisy or sensitive signals (like SIM signals and high-speed digital lines).
- ☑ Optimize placement for minimum length of RF lines.
- ☑ Check the footprint and paste mask designed for SARA-S520BM10 module as illustrated in section 2.12.
- ☑ **VCC** line should be enough wide and as short as possible.
- ☑ Route **VCC** supply line away from RF lines / parts (refer to Figure 23) and other sensitive analog lines / parts.
- ☑ The **VCC** bypass capacitors in the picofarad range should be placed as close as possible to the **VCC** pins, in particular if the application device integrates an internal antenna.
- ☑ Provide an optimal ground connection of the **GND** pins in the area where the internal Satellite Power Amplifier is located (see Figure 24, section 2.2.1.10).
- ☑ Provide a weak ground connection of the **GND** pins in the area where the internal TCXO is located (see Figure 24, section 2.2.1.10).
- ☑ Use as many vias as possible to connect the ground planes on multilayer application board, providing a dense line of vias at the edges of each ground area, in particular along RF and high-speed lines, and along the edges of the application board.
- ☑ Keep routing short and minimize parasitic capacitance on the SIM lines to preserve signal integrity.
- ☑ **USB_D+** / **USB_D-** traces should meet the characteristic impedance requirement (90 Ω differential and 30 Ω common mode) and should not be routed close to any RF line / part.

2.15.3 Antennas checklist

- ☑ Antenna termination should provide 50 Ω characteristic impedance with V.S.W.R at least less than 3:1 (recommended 2:1) on operating bands in deployment geographical area.
- ☑ Follow the recommendations of the antenna producer for correct antenna installation and deployment (PCB layout and matching circuitry).
- ☑ Ensure compliance with any regulatory agency RF radiation requirement, as reported in section 4.2 for FCC United States, in section 4.3 for ISED Canada, in section 4.4 for Europe, etc.
- ☑ Ensure high isolation between the cellular antenna and any other antennas or transmitters present on the end device.
- ☑ Ensure high isolation between the cellular antenna and the Satellite / GNSS antenna (see also section 2.4.4).

3 Handling and soldering

No natural rubbers, no hygroscopic materials or materials containing asbestos are employed.

3.1 Packaging, shipping, storage, and moisture preconditioning

For information pertaining to SARA-S520BM10 reels / tapes, Moisture Sensitivity levels (MSD), shipment and storage information, as well as drying for preconditioning, see the SARA-S520BM10 data sheet [1] and the u-blox package information user guide [14].

3.2 Handling

The SARA-S520BM10 modules are Electro-Static Discharge (ESD) sensitive devices.

Ensure ESD precautions are implemented during handling of the module.

Electro-Static Discharge (ESD) is the sudden and momentary electric current that flows between two objects at different electrical potentials caused by direct contact or induced by an electrostatic field. The term is usually used in the electronics and other industries to describe momentary unwanted currents that may cause damage to electronic equipment.

The ESD sensitivity for each pin of SARA-S520BM10 modules (as Human Body Model according to JESD22-A114F) is specified in the SARA-S520BM10 data sheet [1].

ESD prevention is based on establishing an Electrostatic Protective Area (EPA). The EPA can be a small working station or a large manufacturing area. The main principle of an EPA is that there are no highly charging materials near ESD sensitive electronics, all conductive materials are grounded, workers are grounded, and charge build-up on ESD sensitive electronics is prevented. International standards are used to define typical EPA and can be obtained for example from the International Electrotechnical Commission (IEC) or the American National Standards Institute (ANSI).

In addition to standard ESD safety practices, the following measures should be considered whenever handling the SARA-S520BM10 modules:

- Unless there is a galvanic coupling between the local GND (i.e. the work table) and the PCB GND, then the first point of contact when handling the PCB must always be between the local GND and PCB GND.
- Before mounting an antenna patch, connect the ground of the device.
- When handling the module, do not come into contact with any charged capacitors and be careful when contacting materials that can develop charges (e.g. patch antenna, coax cable, soldering iron).
- To prevent electrostatic discharge through the RF pin, do not touch any exposed antenna area. If there is any risk that such exposed antenna area is touched in a non-ESD protected work area, implement adequate ESD protection measures in the design.
- When soldering the module and patch antennas to the RF pin, make sure to use an ESD-safe soldering iron.

3.3 Soldering

3.3.1 Soldering paste

“No Clean” soldering paste is strongly recommended for SARA-S520BM10 modules, as it does not require cleaning after the soldering process has taken place. The paste listed in the example below meets these criteria.

Soldering paste:	OM338 SAC405 / Nr.143714 (Cookson Electronics)
Alloy specification:	95.5% Sn / 3.9% Ag / 0.6% Cu (95.5% tin / 3.9% silver / 0.6% copper) 95.5% Sn / 4.0% Ag / 0.5% Cu (95.5% tin / 4.0% silver / 0.5% copper)
Melting temperature:	217 °C
Stencil thickness:	150 µm for base boards

The final choice of the soldering paste depends on the approved manufacturing procedures.

The paste-mask geometry for applying soldering paste should meet the recommendations in section 2.12.

☞ The quality of the solder joints should meet the appropriate IPC specification.

3.3.2 Reflow soldering

A convection type-soldering oven is strongly recommended for SARA-S520BM10 modules over the infrared type radiation oven. Convection heated ovens allow precise control of the temperature and all parts will be heated up evenly, regardless of material properties, thickness of components and surface color.

Consider the “IPC-7530A Guidelines for temperature profiling for mass soldering (reflow and wave) processes”. Reflow profiles are to be selected according to the following recommendations.

⚠ Failure to observe these recommendations can result in severe damage to the device!

Preheat phase

Initial heating of component leads and balls. Residual humidity will be dried out. Note that this preheat phase will not replace prior baking procedures.

- Temperature rise rate: max 3 °C/s
  If the temperature rise is too rapid in the preheat phase it may cause excessive slumping.
- Time: 60 ÷ 120 s
  If the preheat is insufficient, rather large solder balls tend to be generated. Conversely, if performed excessively, fine balls and large balls will be generated in clusters.
- End temperature: +150 ÷ +200 °C
  If the temperature is too low, non-melting tends to be caused in areas containing large heat capacity.

Heating/ reflow phase

The temperature rises above the liquidus temperature of +217 °C. Avoid a sudden rise in temperature as the slump of the paste could become worse.

- Limit time above +217 °C liquidus temperature: 40 ÷ 60 s
- Peak reflow temperature: +245 °C

Cooling phase

A controlled cooling avoids negative metallurgical effects of the solder (solder becomes more brittle) and possible mechanical tensions in the products. Controlled cooling helps to achieve bright solder fillets with a good shape and low contact angle.

- Temperature fall rate: max 4 °C/s

☞ To avoid falling off, modules should be placed on the topside of the motherboard during soldering.

The soldering temperature profile chosen at the factory depends on additional external factors like choice of soldering paste, size, thickness and properties of the base board, etc.

⚠ Exceeding the maximum soldering temperature and the maximum liquidus time limit in the recommended soldering profile may permanently damage the module.

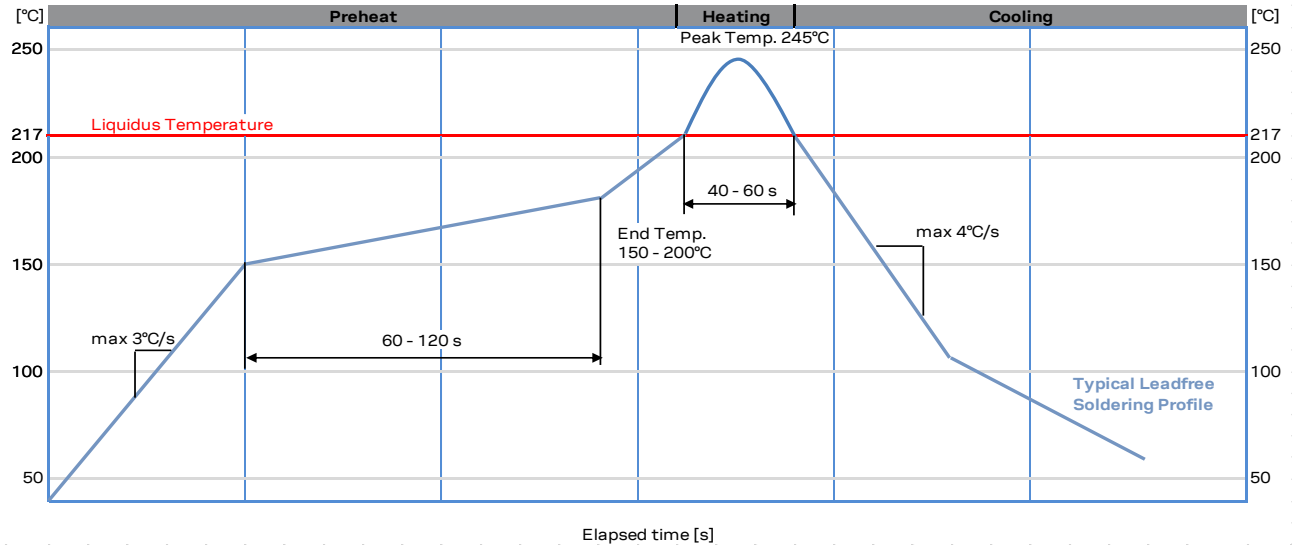

Figure 66: Recommended soldering profile

☞ The modules must not be soldered with a damp heat process.

3.3.3 Optical inspection

After soldering the module, inspect it optically to verify that it is correctly aligned and centered.

3.3.4 Cleaning

Cleaning the modules is not recommended. Residues underneath the modules cannot be easily removed with a washing process.

- Cleaning with water will lead to capillary effects where water is absorbed in the gap between the baseboard and the module. The combination of residues of soldering flux and encapsulated water leads to short circuits or resistor-like interconnections between neighboring pads. Water will also damage the sticker and the ink-jet printed text.
- Cleaning with alcohol or other organic solvents can result in soldering flux residues flooding into the housing, area that is not accessible for post-wash inspections. The solvent will also damage the sticker and the ink-jet printed text.
- Ultrasonic cleaning will permanently damage the module, in particular the quartz oscillators.

For best results, use a “no clean” soldering paste and eliminate the cleaning step after the soldering.

3.3.5 Repeated reflow soldering

Repeated reflow soldering processes and soldering the module upside-down are not recommended.

Boards with components on both sides may require two reflow cycles. In this case, the module should always be placed on the side of the board that is submitted into the last reflow cycle. The reason for this (besides others) is the risk of the module falling off due to the significantly higher weight in relation to other components.

☞ u-blox gives no warranty against damages to the SARA-S520BM10 modules caused by performing more than a total of two reflow soldering processes (one reflow soldering process to mount the SARA-S520BM10 module, plus one reflow soldering process to mount other parts).

3.3.6 Wave soldering

SARA-S520BM10 LGA modules must not be soldered with a wave soldering process.

Boards with combined through-hole technology (THT) components and surface-mount technology (SMT) devices require wave soldering to solder the THT components. No more than one wave soldering process is allowed for a board with a SARA-S520BM10 module already populated on it.

⚠ Performing a wave soldering process on the module can result in severe damage to the device!

☞ u-blox gives no warranty for damages to SARA-S520BM10 modules caused by performing more than a total of two soldering processes (one reflow soldering process to mount SARA-S520BM10 module, plus one wave soldering process to mount other THT parts on the application board).

3.3.7 Hand soldering

Hand soldering is not recommended.

3.3.8 Rework

Rework is not recommended.

☞ Never attempt a rework on the module itself, e.g. replacing individual components. Such actions immediately terminate the warranty.

3.3.9 Conformal coating

Certain applications employ a conformal coating of the PCB using HumiSeal® or other related coating products.

These materials affect the RF properties of the cellular modules and it is important to prevent them from flowing into the module.

The RF shields do not provide 100% protection for the module from coating liquids with low viscosity, therefore care is required in applying the coating.

☞ Conformal coating of the module will void the warranty.

3.3.10 Casting

If casting is required, use viscose or another type of silicon pottant. The OEM is strongly advised to qualify such processes in combination with the cellular modules before implementing this in production.

☞ Casting will void the warranty.

3.3.11 Grounding metal covers

Attempts to improve grounding by soldering ground cables, wick or other forms of metal strips directly onto the EMI covers is done at the customer's own risk. The numerous ground pins should be sufficient to provide optimum immunity to interference and noise.

☞ u-blox gives no warranty for damages to the cellular modules caused by soldering metal cables or any other forms of metal strips directly onto the EMI covers.

3.3.12 Use of ultrasonic processes

The cellular modules contain components which are sensitive to ultrasonic waves. Use of any ultrasonic processes (cleaning, welding etc.) may cause damage to the module.

☞ u-blox gives no warranty for damages to the cellular modules caused by any ultrasonic processes.

4 Approvals

4.1 Product certification approval overview

Product certification approval is the process of certifying that a product has passed all tests and criteria required by specifications, typically called “certification schemes”, which can be divided into:

- Regulatory certifications
  - Country-specific approval required by local government in most regions and countries, as:
    - CE (European Conformity) marking for Europe
    - FCC (Federal Communications Commission) approval for the United States
- Industry certifications
  - Telecom industry-specific approval verifying interoperability between devices and networks:
    - GCF (Global Certification Forum)
    - PTCRB (PCS Type Certification Review Board)
- Operator certifications
  - Operator-specific approvals required by some mobile network operator, such as:
    - AT&T network operator in United States
    - Verizon Wireless network operator in United States

The manufacturer of the end-device that integrates a SARA-S520BM10 module must take care of all certification approvals required by the specific integrating device to be deployed in the market.

The required certification scheme approvals and relative testing specifications applicable to the end-device that integrates a SARA-S520BM10 module differ depending on the country or the region where the integrating device is intended to be deployed, on the relative vertical market of the device, on type, features and functionalities of the whole application device, and on the network operators where the device is intended to operate.

The main approvals of the modules are indicated in the SARA-S520BM10 data sheet [1].

☞ Check the appropriate applicability of the SARA-S520BM10 module’s approvals while starting the certification process of the device integrating the module: the re-use of the u-blox cellular module’s approval can significantly reduce the cost and time to market of the application device certification.

SARA-S520BM10 modules include the capability to configure the device by selecting the operating Mobile Network Operator Profile, Radio Access Technology, Bands. In the AT commands manual [2], see the +UMNOPROF, +URAT, and +UBANDMASK AT commands.

As these configuration decisions are made, u-blox reminds manufacturers of the host application device integrating the SARA-S520BM10 modules to take care of compliance with all the certification approvals requirements applicable to the specific integrating device to be deployed in the market.

☞ It is strongly recommended to configure the module to the applicable MNO profile, RAT, and LTE bands intended for the host end-device and within regulatory compliance.

☞ The certification of the host application device that integrates a SARA-S520BM10 module and the compliance of the host application device with all the applicable certification schemes, directives and standards are the sole responsibility of the host application device manufacturer.

☞ Check the specific settings required by the mobile network operators in use by the host application device, as they may differ from the AT commands factory-programmed settings of the module.

4.2 FCC United States conformity

FCC ID of SARA-S520BM10 modules: XPYUBX24KM03

4.2.1 Integration instructions for host product manufacturers

4.2.1.1 General

This chapter 4.2.1 includes the SARA-S520BM10 modules' integration instructions for host product manufactures according to FCC KDB 996369 D03 v01r01. General FCC guidelines for host product manufactures integrating transmitter modules are available in the FCC KDB 996369 D04 v02.

4.2.1.2 List of applicable FCC rules

FCC United States
47 CFR Part 22 / 24 / 25 / 27 / 90

Table 34: List of FCC rules applicable to SARA-S520BM10 modules

SARA-S520BM10 modular transmitter is only FCC authorized for the specific rule parts listed on the FCC grant. The host product manufacturer is responsible for compliance to any other FCC rules that apply to the host not covered by the modular transmitter grant of certification. See section 4.2.1.10 below regarding additional testing for the host product.

4.2.1.3 Specific operational use conditions

Host product manufacturers are responsible to follow all the integration guidelines included in this manual, and to perform a set of verification testing to ensure the host product complies with any applicable functional and/or conformity requirements.

SARA-S520BM10 modular transmitter must be supplied with operating voltage and current rating specified in the SARA-S520BM10 data sheet [1].

SARA-S520BM10 modular transmitter is an equipment for building-in. Requirements for fire enclosure must be evaluated in the host end product. The clearance and creepage current distances required by the host end product must be withheld when the module is installed. The cooling of the end product shall not negatively be influenced by the installation of the module. Excessive sound pressure from earphones and headphones can cause hearing loss. No natural rubbers, no hygroscopic materials nor materials containing asbestos are employed.

See RF exposure considerations section 4.2.1.6 below for fixed, mobile, and portable use conditions, operation in conjunction with any other transmitter, and maximum gain of the system antenna.

Changes or modifications made to this device that are not expressly approved by u-blox could void the user's authority to operate the equipment.

Host product manufacturers are responsible to include any applicable restrictions imposed by FCC rules, any other applicable notices, or regulatory statements in host's manual for the end-user.

4.2.1.4 Limited module procedures

Not applicable, as the SARA-S520BM10 modular transmitter is granted with FCC Single Modular Approval rather than a Limited Single Modular Approval.

4.2.1.5 Trace antenna designs

Manufacturers of mobile or fixed devices incorporating SARA-S520BM10 modular transmitter are authorized to use the FCC Grant of the module for their own host products if, as per FCC KDB 996369, the antenna trace design implemented on the host PCB is electrically equivalent to the antenna trace design implemented on the u-blox host printed circuit board used for regulatory type approvals of the modular transmitter described in details in section 2.4.7.

Other additional guidelines for RF design are available in section 1.7.1 / 1.7.2 and whole section 2.4.

Guidelines regarding test procedures for design verification and validation with the aim of ensuring compliance with any applicable functional and/or conformity requirements are included in section 5.1.

Guidelines regarding production test procedures are included in section 5.2.

In case of antenna trace design change, an FCC Class II Permissive Change application is required to be filed by the grantee, or the host manufacturer can take responsibility through the change in FCC ID (new application) procedure followed by an FCC Class II Permissive Change application.

4.2.1.6 RF exposure considerations

SARA-S520BM10 modular transmitter complies with FCC radiation exposure limits prescribed for an uncontrolled environment for fixed and mobile use conditions. Manufacturers of mobile or fixed devices incorporating the modular transmitter are authorized to use the FCC Grants of the modular transmitter for their own final products according to the conditions referenced in the certificates.

SARA-S520BM10 modular transmitter should be installed and operated with a minimum distance of 20 cm between the radiator and the body of the user or nearby persons. Manufacturers of portable applications incorporating the SARA-S520BM10 modules are required to have their final product evaluated and tested, applying for their own FCC Grant related to the specific portable device, or executing an FCC Class II Permissive Change application. This is mandatory to meet the SAR requirements for portable devices, with the modular transmitter installed in host products intended to be operated with less than 20 cm between the radiator and the body of the user or nearby persons.

SARA-S520BM10 modular transmitter must not be co-located or operating in conjunction with any other antenna or transmitter except in accordance with FCC procedures and as authorized in the modular transmitter FCC certification filing.

The gain of the system cellular antenna(s) used for the SARA-S520BM10 modular transmitter (i.e. the combined transmission line, connector, cable losses and radiating element gain) must not exceed the value specified in the FCC Grant for mobile and/or fixed operating configurations

4.2.1.7 Antennas

SARA-S520BM10 surface-mounted LGA modular transmitter includes the **ANT** pad, consisting in the RF port of the module that can be connected through an RF antenna trace designed on the host PCB to any antenna compliant with any appliable rules for RF exposure or any other.

4.2.1.8 Label and compliance information

If the FCC Grant of the SARA-S520BM10 modular transmitter can be used for the final host product, as the conditions referenced in the certificates and in this chapter 4.2.1 are met, the FCC Label of the module shall be visible from the outside, or the host device shall bear a second label stating:

Contains FCC ID: XPYUBX24KM03

See the general FCC guidelines for labeling and other information required to be provided to users of RF devices available in the KDB Publication 784748.

4.2.1.9 Information on test modes and additional testing requirements

The host product manufacturer is responsible for compliance to any other FCC rules that apply to the host not covered by the modular transmitter grant of certification. Compliance of the host product with RF regulatory rules defined by the FCC can be verified using a radio communication tester (callbox), as for example the Rohde & Schwarz CMW500, or any equivalent equipment for multi-radio technology signaling conformance tests.

Test modes should also take into consideration different operational conditions for a stand-alone modular transmitter in a host product, as well as for multiple simultaneously transmitting modules or other transmitters co-located in a host product.

Consider involving an accredited testing laboratory to verify compliance with RF regulatory rules.

Additional guidance for testing host products is given in the FCC KDB Publication 996369 D04.

4.2.1.10 Additional testing, Part 15 Subpart B disclaimer

SARA-S520BM10 modular transmitter is only FCC authorized for the specific rule parts listed on the FCC grant (see section 4.2.1.2). The host product manufacturer is responsible for compliance to any other FCC rules that apply to the host not covered by the modular transmitter grant of certification.

This device complies with Part 15 of the FCC rules Operation is subject to the following two conditions:

- This device may not cause harmful interference
- This device must accept any interference received, including interference that may cause undesired operation

Part 15 limits of the FCC Rules for a Class B digital device are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:

- Reorient or relocate the receiving antenna
- Increase the separation between the equipment and receiver
- Connect the device into an outlet on a circuit different from that to which the receiver is connected
- Consultant the dealer or an experienced radio/TV technician for help

SARA-S520BM10 modular transmitter is Part 15 Subpart B compliant, but the final host product still requires Part 15 Subpart B compliance testing with the modular transmitter installed.

4.3 ISED Canada conformity

ISED Canada certification number of SARA-S520BM10 modules: 8595A-UBX24KM03

4.3.1 Innovation, Science and Economic Development Canada notices

This device contains licence-exempt transmitter(s)/receiver(s) that comply with Innovation, Science and Economic Development (ISED) Canada's licence-exempt RSS(s). Operation is subject to the following two conditions:

1. This device may not cause harmful interference.
2. This device must accept any interference received, including interference that may cause undesired operation.

Radio Frequency (RF) Exposure Information

This equipment complies with radiation exposure limits prescribed for an uncontrolled environment for fixed and mobile use conditions. This equipment should be installed and operated with a minimum distance of 20 cm between the radiator and the body of the user or nearby persons. This transmitter must not be co-located or operating in conjunction with any other antenna or transmitter except as authorized in the certification of the product.

The radiated output power of the SARA-S520BM10 module is below the ISED Canada radio frequency exposure limits. The SARA-S520BM10 module should be used in a manner such that the potential for human contact during normal operation is minimized.

This device has been evaluated and shown compliant with the Canadian RF Exposure limits under mobile exposure conditions (antennas are greater than 20 cm from a person's body).

This device has been certified for use in Canada. Status of the listing in the Innovation, Science and Economic Development (former Industry Canada) Radio Equipment List can be found at the address: https://sms-sgs.ic.gc.ca/equipmentSearch/searchRadioEquipments?execution=e1s1&lang=en_CA

Additional Canadian information on RF exposure also can be found at the following web address: frequently-asked-questions-faq-radiofrequency-rf-energy-and-health

The gain of the system antenna(s) used for the SARA-S520BM10 modules (i.e. the combined transmission line, connector, cable losses and radiating element gain) must not exceed the value stated in the ISED Canada Grant for mobile and fixed or mobile operating configurations

IMPORTANT:

Manufacturers of portable applications incorporating the modules are required to have their final product certified and apply for their own ISED Canada Certificate related to the specific portable device. This is mandatory to meet the SAR requirements for portable devices.

Manufacturers of mobile or fixed devices incorporating the SARA-S520BM10 modules are authorized to use the ISED Canada Certificates of the SARA-S520BM10 modules for their own final products according to the conditions referenced in the certificates.

The Innovation, Science and Economic Development Canada (former Industry Canada) label shall in the above case be visible from the outside, or the host device shall bear a second label stating:

Contains IC: 8595A-UBX24KM03

Changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate the equipment.

ISED Canada requires the user to be notified that any changes or modifications made to this device that are not expressly approved by u-blox could void the user's authority to operate the equipment.

4.3.2 Avis d'Innovation, Sciences et Développement Économique Canada

L'émetteur/récepteur exempt de licence contenu dans le présent appareil est conforme aux CNR d'Innovation, Sciences et Développement Économique Canada (ISDE) applicables aux appareils radio exempts de licence. L'exploitation est autorisée aux deux conditions suivantes:

1. L'appareil ne doit pas produire de brouillage;
2. L'appareil doit accepter tout brouillage radioélectrique subi, même si le brouillage est susceptible d'en compromettre le fonctionnement.

Informations concernant l'exposition aux fréquences radio (RF)

La puissance de sortie émise par l'appareil de sans-fil SARA-S520BM10 module est inférieure à la limite d'exposition aux fréquences radio d'ISDE Canada. Utilisez l'appareil de sans-fil module de façon à minimiser les contacts humains lors du fonctionnement normal.

Ce périphérique a été évalué et démontré conforme aux limites d'exposition aux fréquences radio (RF) d'IC lorsqu'il est installé dans des produits hôtes particuliers qui fonctionnent dans des conditions d'exposition à des appareils mobiles (les antennes se situent à plus de 20 centimètres du corps d'une personne).

Ce périphérique est homologué pour l'utilisation au Canada. Pour consulter l'entrée correspondant à l'appareil dans la liste d'équipement radio (Radio Equipment List) d'ISDE Canada rendez-vous sur: https://sms-sgs.ic.gc.ca/equipmentSearch/searchRadioEquipments?execution=e1s1&lang=fr_CA

Pour des informations supplémentaires concernant l'exposition aux RF au Canada rendez-vous sur: questions-souvent-posees-qui-concerne-lenergie-radioelectrique-sante

IMPORTANT:

Les fabricants d'applications portables contenant les modules de la SARA-S520BM10 doivent faire certifier leur produit final et déposer directement leur candidature pour une certification FCC ainsi que pour un certificat ISDE Canada délivré par l'organisme chargé de ce type d'appareil portable. Ceci est obligatoire afin d'être en accord avec les exigences SAR pour les appareils portables.

Tout changement ou modification non expressément approuvé par la partie responsable de la certification peut annuler le droit d'utiliser l'équipement.

4.4 European Conformity

The SARA-S520BM10 modules have been evaluated against the essential requirements of the Radio Equipment Directive 2014/53/EU (RED). To satisfy the essential requirements of the RED, the modules are compliant with the following standards:

- Radio Spectrum Efficiency (Article 3.2):
  - EN 301 426
  - EN 301 908-1
  - EN 301 908-13
  - EN 303 413
- Electromagnetic Compatibility (Article 3.1b):
  - EN 301 489-1
  - EN 301 489-19
  - EN 301 489-20
  - EN 301 489-52
- Health and Safety (Article 3.1a)
  - EN 62368-1
  - EN 62311

Radiofrequency radiation exposure information

This equipment complies with radiation exposure limits prescribed for an uncontrolled environment for fixed and mobile use conditions. This equipment should be installed and operated with a minimum distance of 20 cm between the radiator and the body of the user or nearby persons. This transmitter must not be co-located or operating in conjunction with any other antenna or transmitter except as authorized in the certification of the product.

The gain of the system antenna(s) used for SARA-S520BM10 modules (i.e. combined transmission line, connector, cable losses and radiating element gain) must not exceed the values stated in the Declaration of Conformity of the modules, for mobile and fixed or mobile operating configurations

CE mark note

The conformity assessment procedure for the SARA-S520BM10 modules, referred to in Article 17 and detailed in Annex II of Directive 2014/53/EU, has been followed.

Thus, the following marking is included in the product:

CE

Notes for Great Britain / United Kingdom

☞ The UK Government Department for Business and Trade has announced an indefinite extension to the use of CE marking for businesses, beyond December 2024, for many products. For more details, see: uk-government-announces-extension-of-ce-mark-recognition-for-businesses

☞ For guidance about using the UKCA marking, see: using-the-ukca-marking

4.5 ORBCOMM conformity

Products that integrate SARA-S520BM10 modules require type approval from ORBCOMM before being authorized to operate on the satellite network.

☞ We recommend contacting ORBCOMM to get details about the ORBCOMM type approval process.

Green lane process

If the product integrates the pre-certified SARA-S520BM10 modules and an ORBCOMM-specified antenna, without any change in the antenna or cable, the Type Approval process will be granted in a simplified process.

☞ We recommend contacting ORBCOMM to get the list of pre-certified Satellite antennas specified by ORBCOMM for the Satellite RF operations.

Full type approval process

Final products integrating the SARA-S520BM10 modules may require full ORBCOMM Type Approval tests if any of the following apply:

- The final product uses a module that has been modified.
- The final product uses a pre-certified antenna that has been modified or uses an antenna that is not pre-certified.

5 Product testing

5.1 Validation testing and qualification

SARA-S520BM10 modules are validated and tested by u-blox in the operating conditions and in certain integration, but not all the specific characteristics of the host application end-product integrating the module can be validated and tested by u-blox.

SARA-S520BM10 modules are also qualified by u-blox according to u-blox reliability stress tests policy, based on AEC-Q104 standard; but the specific characteristics of the host application end-product integrating the module cannot be qualified by u-blox.

Therefore, and to be on the safe side, u-blox recommends integrators of SARA-S520BM10 modules to validate, verify, qualify and test in details the host product integrating the SMD module considering all the possible aspects, to make sure that the specific characteristics of the host application do not lead to reduced / non-performance of SARA-S520BM10 modules.

Host product manufacturers are responsible to follow all the integration guidelines included in this manual, and to perform a set of verification testing to ensure the host end-product complies with applicable functional and/or conformity requirements.

Carefully validate the antennas RF circuits implemented in the host product for the module, as they may affect compliance with applicable RF conformity requirements.

The 50 Ω characteristic impedance of the antenna trace design on a host printed circuit board can be verified using a Vector Network Analyzer, as done on the u-blox host PCB, with calibrated RF coaxial cable soldered at the pad corresponding to RF input/output of the module and with the transmission line terminated to a 50 Ω load at the 50 Ω SMA female connector.

Compliance of the design with RF regulatory rules defined by the FCC, ISED, RED, etc. can be verified using a radio communication tester (callbox) as the Rohde & Schwarz CMW500, or any equivalent equipment for multi-technology signaling conformance tests.

Carefully validate the VCC power supply circuit implemented in the host product for the module, as the specific characteristics of the power supply circuit may affect compliance with applicable functional and/or conformity requirements.

Adequateness of the power supply circuit capability can be checked by forcing the module to transmit at the maximum power level in the supported radio access technologies using a radio communication tester (callbox) as the Rohde & Schwarz CMW500 or any equivalent equipment.

Carefully validate the SIM interface circuit implemented in the host product for the module, check particularly rise times of the signals, as the external circuit design may affect compliance with applicable functional and/or specification requirements.

Carefully validate any interface circuit connected to the module as implemented in the host product, check particularly the power-on, power-off and reset circuits with also any related switch-on, switch-off and reset procedure, the communication interfaces (as UARTs, USB, I2C), and any other circuit designed in the host product in combination with any other interface of the module (as GPIOs, etc.), as the external design implemented in the host product may affect compliance with applicable functional requirements.

☞ The validation, verification, qualification, and testing of the application host device integrating a SARA-S520BM10 module and the compliance of the application host device with all the applicable functional and/or conformity specifications and requirements are under the sole responsibility of the application host device manufacturer.

5.2 Production testing

5.2.1 u-blox in-line production tests

u-blox focuses on high quality for its products. All units produced are tested automatically in all their interfaces along the production line. Stringent quality control processes have been implemented in the production line. Defective units are analyzed in detail to improve production quality.

This is achieved with automatic test equipment (ATE) in the production line, which logs all production and measurement data. A detailed test report for each unit can be generated from the system. The following Figure 67 illustrates the typical automatic test equipment (ATE) in a production line.

The following typical tests are among the production tests.

- Digital self-test (firmware download, flash firmware verification, IMEI programming)
- Measurement of voltages and currents
- Adjustment of ADC measurement interfaces
- Functional tests (serial interface communication, SIM card communication)
- Digital tests (GPIOs and other interfaces)
- Measurement and calibration of RF characteristics in all supported bands
- Verification of the RF characteristics after calibration

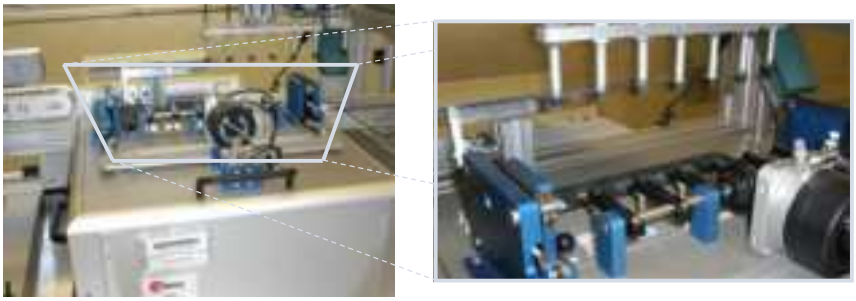

Figure 67: Automatic test equipment for module tests

5.2.2 Production test parameters for OEM manufacturers

5.2.2.1 General guidelines for production testing

☞ AT commands reported in this section are only for example. For further details, see the AT commands manual [2].

Because of the testing done by u-blox (with 100% coverage), an OEM manufacturer does not need to repeat the firmware tests or measurements of the module RF performance or tests over analog and digital interfaces in their production test.

However, an OEM manufacturer should focus on:

- Module assembly on the application device, verify that:
  - The soldering and handling process did not damage the module components,
  - All module pins are well soldered on the device board,
  - There are no short circuits between pins
- Component assembly on the application device, verify that:
  - Communication with the host can be established,
  - The interfaces between the module and device are working,
  - The RF interfaces including the antenna/s are working

Dedicated tests can be implemented to check the device. For example, the consumption measured in a specified status can detect a short circuit if compared with a “Golden Device” result.

In addition, module AT commands can be used to perform functional tests on the digital interfaces. For example:

- Communication with the host can be checked by AT command,
- Communication with the SIM card/chip by the +CPIN read command,
- Communication with external I2C devices by dedicated I2C AT commands,
- GPIO functionality by the dedicated +UGPIOC AT command, etc.

☞ Please contact the u-blox office or sales representative nearest you for further guidelines about OEM production testing guidelines.

5.2.2.2 Functional production tests providing GNSS RF operation

The best way to test the GNSS RF functionality is with the use of a GNSS simulator, as it assures reliable and constant signals at every measurement. Spirent, Rohde & Schwarz, and Orolia amongst other manufacturers offer such devices.

Guidelines for GNSS RF functionality tests:

3. Connect a GNSS generator to the OEM product.
4. Choose the power level in a way that the “Golden Device” would report a C/No ratio of 38-40 dBHz.
5. Power up the DUT (Device Under Test) and allow enough time for the acquisition.
6. Read the C/No value from the NMEA GSV or any UBX message reporting it (e.g. with u-center).
7. Compare the results to a “Golden Device”.

5.2.2.3 Persistent configurations

The modules are delivered by u-blox with predefined factory-programmed settings that can be changed using AT commands according to application-specific requirements. Some settings are persistent, stored in the module's non-volatile memory, and re-used at any subsequent reboot. Among these, for example, there are the UART interfaces’ baud rate, the greeting text, the MNO profile, the APN for internet connectivity, etc.

After verifying the proper assembly of the module and related parts on the application device, execute a persistent configuration setting phase in OEM production line, configuring the module according to the intended use in the specific application, as the persistent configurations are intended to be set only once and then re-used at any subsequent reboot.

Appendix

A Glossary

Abbreviation	Definition
ADC	Analog to Digital Converter
AR	Axial Ratio
AT	AT Command Interpreter Software Subsystem, or attention
BBR	Battery-Backed RAM
BeiDou	Chinese satellite navigation system
BJT	Bipolar Junction Transistor
C/No	Carrier to Noise ratio
C2PC	Class II Permissive Change
C4PC	Class IV Permissive Change
Cat	Category
CE	European Conformity
CoAP	Constrained Application Protocol
CTS	Clear To Send
DC	Direct Current
DCD	Data Carrier Detect
DCE	Data Communication Equipment
DDC	Display Data Channel interface
DL	Down-Link (Reception)
DRX	Discontinuous Reception
DSR	Data Set Ready
DTE	Data Terminal Equipment
DTLS	Datagram Transport Layer Security
DTR	Data Terminal Ready
eDRX	Extended Discontinuous Reception
EMC	Electro-Magnetic Compatibility
EMI	Electro-Magnetic Interference
ESD	Electro-Static Discharge
ESR	Equivalent Series Resistance
ETSI	European Telecommunications Standards Institute
E-UTRA	Evolved Universal Terrestrial Radio Access
FCC	Federal Communications Commission United States
FDD	Frequency Division Duplex
FOAT	Firmware Over AT commands
FOTA	Firmware Over The Air
FW	Firmware
Galileo	European satellite navigation system
GCF	Global Certification Forum
GEO	Geosynchronous Equatorial Orbit
GLONASS	GLObal Navigation Satellite System (Russian satellite navigation system)
GNSS	Global Navigation Satellite System
GPIO	General Purpose Input Output

Abbreviation	Definition
GPS	Global Positioning System
GSM	Global System for Mobile communication
HBM	Human Body Model
HDLC	High-level Data Link Control
HTTP	HyperText Transfer Protocol
HW	Hardware
I2C	Inter-Integrated Circuit interface
IC	Integrated Circuit
IDP	IsatData Pro
IEC	International Electrotechnical Commission
IP	Internet Protocol
IPC	Institute of Printed Circuits
ISED	Innovation, Science and Economic Development Canada
ISO	International Organization for Standardization
ITU	International Telecommunication Union
LDO	Low-Dropout
LED	Light Emitting Diode
LGA	Land Grid Array
LNA	Low Noise Amplifier
LPWA	Low Power Wide Area
LTE	Long Term Evolution
LwM2M	Open Mobile Alliance Lightweight Machine-to-Machine protocol
M2M	Machine-to-Machine
MOSFET	Metal-Oxide-Semiconductor Field-Effect Transistor
MQTT	Message Queuing Telemetry Transport
MQTT-SN	Message Queuing Telemetry Transport for Sensor Networks
NAS	Non Access Stratum
NB	Narrow Band
NTC	Negative Temperature Coefficient
OGx	Orbcomm Generation X
OTA	Over The Air
PA	Power Amplifier
PCN	Product Change Notification / Sample Delivery Note / Information Note
PFM	Pulse Frequency Modulation
PIFA	Planar Inverted-F Antenna
PPS	Pulse Per Second
PSM	Power Saving Mode
PTCRB	PCS Type Certification Review Board
PTW	Paging Time Window (during eDRX cycles)
PWM	Pulse Width Modulation
QZSS	Quasi-Zenith Satellite System
RAT	Radio Access Technology
RF	Radio Frequency
RHCP	Right-Hand Circular Polarization
RI	Ring Indicator
RSSI	Received Signal Strength Indication

Abbreviation	Definition
RSVD	Reserved
RTC	Real Time Clock
RTS	Request To Send
Rx	Receiver
SAIF	Sub-meter-class Augmentation with Integrity Function
SAW	Surface Acoustic Wave
SBAS	Satellite-Based Augmentation System
SDIO	Secure Digital Input Output
SMA	Sub-Miniature version A
SMD	Surface Mounting Device
SMT	Surface Mount Technology
SP4T	Single-Pole, 4-Throws
SPI	Serial Peripheral Interface
SQI	Serial Quad Input/Output
SRF	Self-Resonant Frequency
TBD	To Be Defined
TCXO	Temperature-Controlled Crystal Oscillator
THT	Through-Hole Technology
TIS	Total Isotropic Sensitivity
TLS	Transport Layer Security
TP	Test Point
TRP	Total Radiated Power
Tx	Transmitter
UART	Universal Asynchronous Receiver-Transmitter
UDP	User Datagram Protocol
UICC	Universal Integrated Circuit Card
UL	Up-Link (Transmission)
URC	Unsolicited Result Code
VSWR	Voltage Standing Wave Ratio

Related documentation

[1] u-blox SARA-S520BM10 data sheet, UBXDOC-686885345-1875
[2] u-blox SARA-S520BM10 AT commands manual, UBXDOC-686885345-2034
[3] Universal Serial Bus revision 2.0 specification, https://www.usb.org/
[4] ITU-T recommendation V.24 – 02-2000 – List of definitions for interchange circuits between Data Terminal Equipment (DTE) and Data Circuit-terminating Equipment (DCE), http://www.itu.int/rec/T-REC-V.24-200002-I/en
[5] 3GPP TS 27.007 – AT command set for User Equipment (UE)
[6] 3GPP TS 27.005 – Use of Data Terminal Equipment – Data Circuit terminating; Equipment (DTE – DCE) interface for Short Message Service (SMS) and Cell Broadcast Service (CBS)
[7] 3GPP TS 27.010 – Terminal Equipment to User Equipment (TE-UE) multiplexer protocol
[8] u-blox mux implementation application note, UBX-13001887
[9] I2C-bus specification and user manual – UM10204, https://www.nxp.com/
[10] GSM Association TS.09 – Battery Life Measurement and Current Consumption Technique, https://www.gsma.com/newsroom/wp-content/uploads//TS.09-v12.pdf
[11] 3GPP TS 36.521-1 – Evolved Universal Terrestrial Radio Access; User Equipment conformance specification; Radio transmission and reception; Part 1: Conformance Testing
[12] 3GPP TS 36.521-2 – Evolved Universal Terrestrial Radio Access (E-UTRA); User Equipment conformance specification; Radio transmission and reception; Part 2: Implementation Conformance Statement (ICS)
[13] 3GPP TS 36.523-2 – Evolved Universal Terrestrial Radio Access (E-UTRA) and Evolved Packet Core (EPC); User Equipment conformance specification; Part 2: Implementation Conformance Statement (ICS)
[14] u-blox package information user guide, UBX-14001652

☞ For regular updates to u-blox documentation and to receive product change notifications, register on our homepage (www.u-blox.com).

Revision history

Revision	Date	Name	Comments
R01	23-Oct-2024	psca / sses	Initial release

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For further support and contact information, visit us at www.u-blox.com/support.