FCC ID: PIYJ8865-06A4R

Technical Description :

The brief circuit description is listed as follows :
- Q26 and associated circuit act as 49.860 MHz Super-regenerative Receiver.
- U1(SPRC206A) and associated circuit act as Decoder.
- U2, U3 and associated circuit act as IR Receiving Circuit.
- U4(SPC11192A) and associated circuit act as Sound and Leg/Arm/Base Controller.
- U5(SPC11024A) and associated circuit act as Leg/Arm Location Detector.
- U6(SPES204B) acts as Mode Controller.
- U7 and associated circuit act as Voltage Regulator.
- Q7, Q8, Q16, Q17, Q24, Q25 and associated circuit act as Base Motor Driver.
- Q5, Q6, Q13, Q14, Q22, Q23 and associated circuit act as Leg Motor Driver.
- Q1, Q2, Q9, Q10, Q18, Q19 and associated circuit act as Left Arm Motor Driver.
- Q3, Q4, Q11, Q12, Q20, Q21 and associated circuit act as Right Arm Motor Driver.
- S13, S14 and S15 act as Mode Keys.
- S2 – S10 acts as Left Arm, Right Arm and Leg Movement Control Keys.
- S12 acts as Base Motor Spin Angle Control Key.
- S11 acts as Music ON/OFF Key.

Antenna Used :

An integral antenna has been used.

DATA SHEET

SUNPLUS

SPRC205A/SPRC206A

5-Function Remote Control Encoder/Decoder

Preliminary

MAR. 14, 2005

Version 0.3

FIVE FUNCTIONS REMOTE CONTROL ENCODER/DECODER PAIRS

1. GENERAL DESCRIPTION

These two devices are especially designed is use as paired encoder/decoder in remote control (RC) applications.

The SPRC205A, a RC encoder, is able to encode five lines of binary information into a serial bit-stream data. When any of the 5-line information is activated, built-in crystal oscillator and power amplifier will be enabled to deliver the encoded bit-stream data. After the 5-line information becomes inactive, the SPRC205A will transmit additional fifteen data frames to increase transmission reliability.

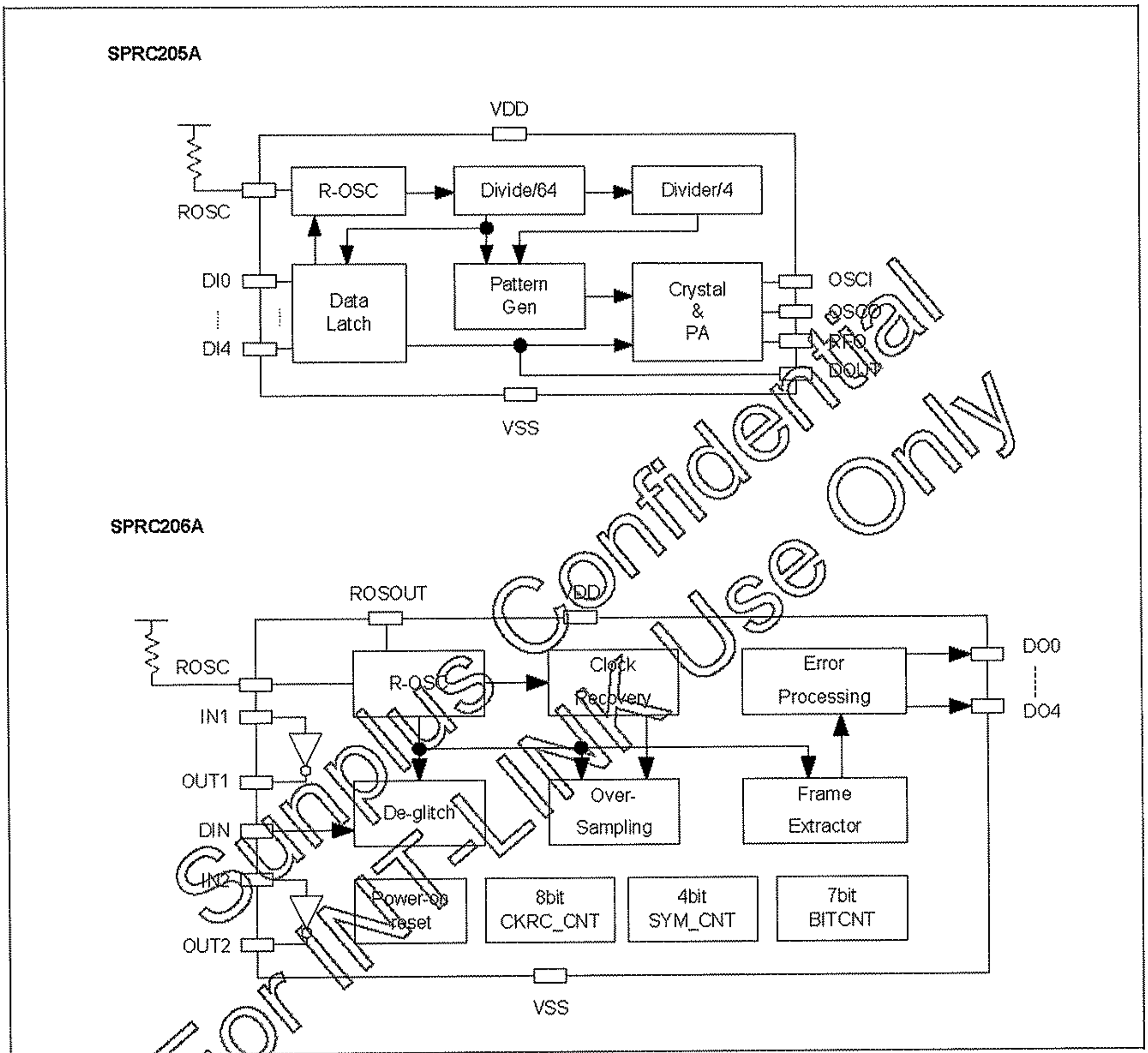
The SPRC206A is a remote control decoder, which decodes the serial bit-stream data received from the SPRC205A and interprets the 5-line information as 5-bit output data to control the corresponding external component. The SPRC206A will be activated only when two consecutive and equal frames are received.

With SUNPLUS state-of-the-art technology and strong support, SPRC205A and SPRC206A are the simplest and most suitable products for your RC products.

2. FEATURES

- Operating voltage
  - 2.2V - 5.5V operation
- Built-in R-oscillator (a 5% resistor required)
- Low standby and operating current
  - $I_{STBY,SPRC206A}$ < 1.0µA, R-oscillator stops
  - $I_{OPERATE,SPRC205A}$ < 15mA, R-oscillator free run, crystal & PA on
  - $I_{OPERATE,SPRC206A}$ < 100µA, R-oscillator free run
- Built-in power on reset
- Built-in Crystal & PA in SPRC205A
- 5-function I/O pins
- $2^5 = 32$ encoding in SPRC205A
- Variable frame rates controlled by external resistor

3. BLOCK DIAGRAM



5. FUNCTIONAL DESCRIPTIONS

5.1. Frame Format

Preamble						PO	E	D0	D1	D2	D3	D4
P	P	P	P	P	P	A/I	A/I	A/I	A/I	A/I	A/I	A/I

Preamble field: 6 preamble fields

PO field: Even parity check field

E field: Frame polarity indication field; frames are transmitted in positive/negative sequence.

Data field: 5 data fields

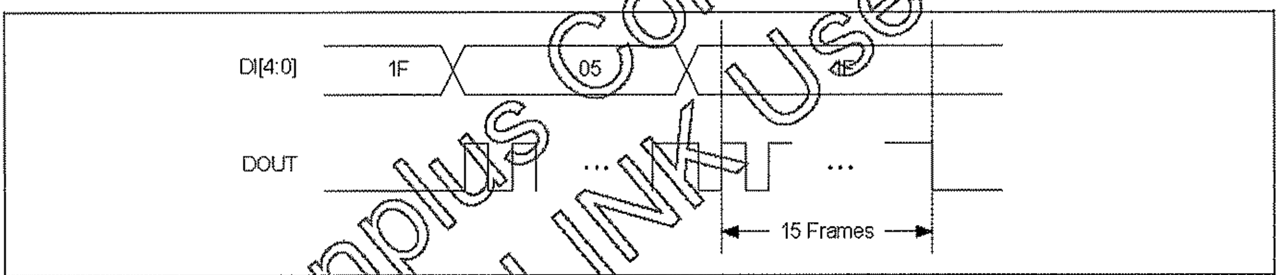
P pattern: encoded as 101

A pattern: encoded as 100

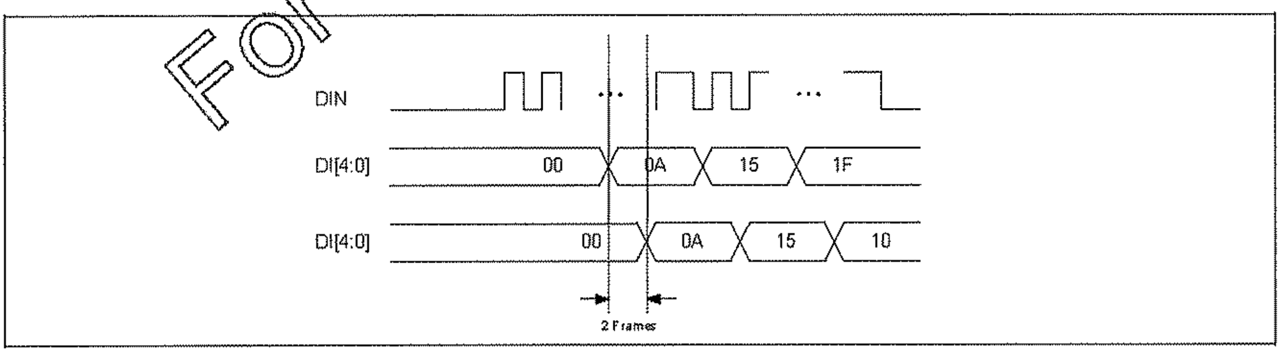
I pattern: encoded as 110

5.2. Operation

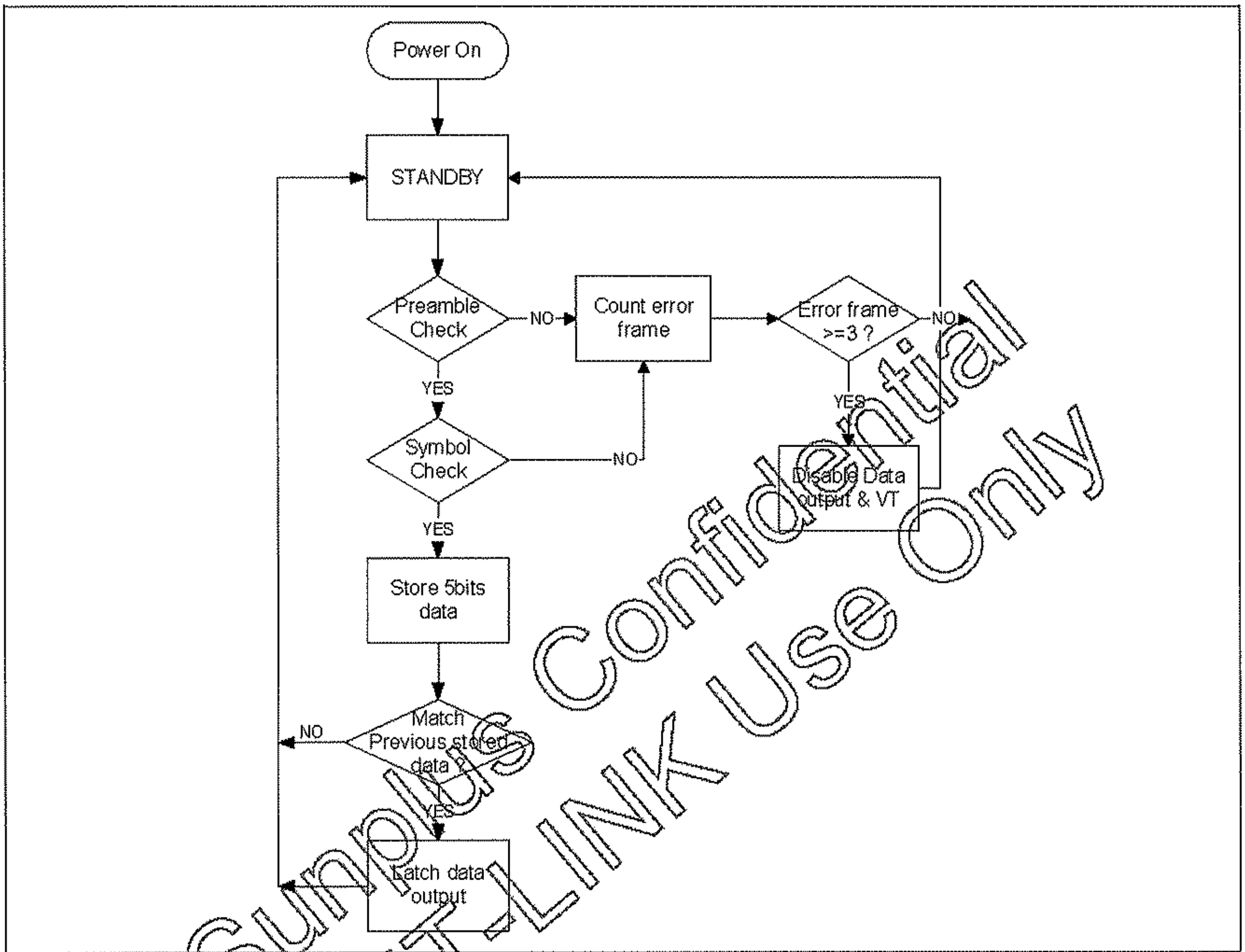
The SPRC205A encodes 5-function information into 2^5 series of bit-stream data and transmits the encoded data stream via RFO when any of the 5-function I/Os is activated. The cycle will repeat until all 5-function I/Os become inactive. After these 5-function I/Os become inactive, SPRC205A will transmit another 15 all-zero frames to inform SPRC206A returning to disabled state. The transmitting timing is shown as follows:



The SPRC206A is able to receive serial bit-stream data transmitted from SPRC205A and decode the data fields as 5-bits data output. Any signal on DIN pin will activate SPRC206A to decode the incoming data. When SPRC206A receives two consecutive, correct and equal frames, DO[4:0] is able to control the external component. The DO[1,0] and DO[3:2] are exclusive to each other; that is, DO[1:0] and DO[3:2] cannot be activated at the same time. The receiving timing is shown below:



5.3. Decoder Flow Chart



After power on, it is reset at STANDBY state. When the signal on DIN is received by SPRC206A, it will check the incoming data frame structure. If preamble or data field errors occur, it will back to STANDBY state to check the next frame. If the receiving frame structure passes the preamble and symbol checks, the 5-bit data is stored and then compared to the previous stored 5-bits data. If the present data matches the previous data, DO[4:0] is active and it is back to STANDBY and ready to check the next frame.

5.4. R-oscillator

Both SPRC205A and SPRC206A have built in R-oscillator. Users need only one resistor (or a capacitor if needed) to implement the clock input and to change the frame rate by replacing different resistor.

Frame rate = F_{OSC} / 64 / 33

In addition, the SPRC206A built-in a Clock Recovery block to automatically adjust the ratio of data rate to clock rate. The only limitation is using a 5% accuracy resistor is required in SPRC205A and SPRC206A.

5.5. Super Regeneration Amplifier

The SPRC206A features two inverter inputs and outputs as pins. The two inverters can be used for amplifier of the Super-Regeneration RF receiver data output. Users can change the two inverters' gain by adjusting external resistor and capacitor.

DATA SHEET

SUNPLUS

SPES204B

easy-to-use SOUNDPLUS

Preliminary

MAY. 06, 2003

Version 0.2

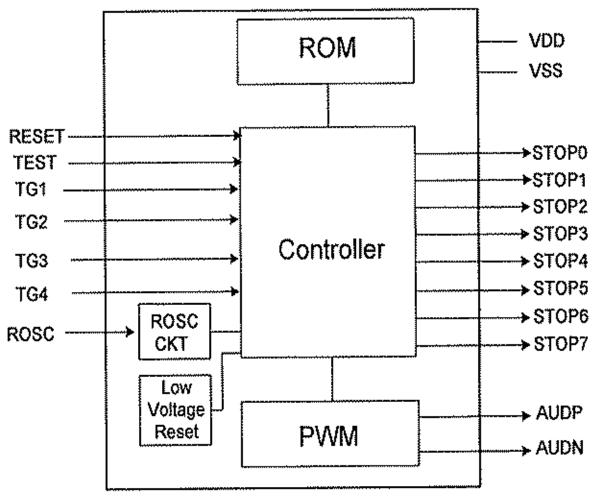
easy-to-use SOUNDPLUS

1. GENERAL DESCRIPTION

The easy-to-use SOUNDPLUS II (SPESII) is an enhanced version of easy-to-use SOUNDPLUS (SPES). Many features such as infrared Red (IR) have been added in SPES II to increase its capability and performance. One of the most significant features in SPES II is that no complex program structure is necessary. With only nine instructions and six registers, SPES II is capable of driving sophisticated tasks and playing realistic sound with simple program structure. Programmer can easily implement application rapidly and increase productivity efficiently.

The SPES204B, one of the SPES II families, stores up to 4 seconds of sound data (@ 6.0KHz sample rate). It also contains four trigger pins, eight output pins, PWM audio output, and five LED flash alternations. To assure the system reliability, a watchdog and a Low Voltage Reset (LVR) are also built in for monitoring possible critical conditions. With the high cost/performance ratio, SPES204B is one of the most suitable engines in the industry for vocal products.

2. BLOCK DIAGRAM



3. FEATURES

- 16KB ROM SIZE
- Programmable speech synthesizer
- Operating voltage:
  - 2.4V - 5.5V for 4.0MHz operating clock
  - 3.6V - 5.5V for 6.0MHz operating clock
- 4 direct trigger inputs that can be extended to 36 matrix key
- Up to 8 programmable outputs
- Programmable power on initialization
- 256 voice group entries available
- Mask options: Trigger input debounce time from 5ms to 35ms
- Flexible functions through the following:
  - LD (load), JP (jump) commands
  - 6 registers: R0, R1, R2, R3, EN, STOP
  - Conditional instructions
  - Speech equation
  - END instruction
  - Local repeat setting
  - Output frequency and LED flash type setting
- Approx. 4 sec. speech (6.0KHz sample rate)
- Low voltage reset function
- Watchdog function
- A pair of PWM outputs
- Flexible functions as the follows:
  - Interrupt or non-interrupt for rising or falling edge of each trigger.
  - Eight programmable playing modes:
    - One shot
    - Level hold
    - Single-cycle level hold
    - Complete-cycle level hold
    - Sequence
    - Level-Auto
    - Random
    - Non-retrigger
  - Stop signal output setting
- Each voice section provides
  - Programmable sampling frequency:
    - 2K to 10K for 4.0MHz operating clock
    - 2K to 15K for 6.0MHz operating clock
  - Five LED flash type : On, Off, Alternatively, Synchronous, Volume-controlled
  - LED: programmable
- Infrared Red (IR) communication Function
- Play Speech with tags. Seven different tags are available

5. FUNCTIONAL DESCRIPTIONS

5.1. Instruction Sets

Nine instructions involve *LD, JP, LSR, ADD, SUB, AND, ORR, EOR, and END*. "LD" represents LOAD and "JP" indicates JUMP. "LSR" shifts a register's value one bit to the right. "ADD" and "SUB" are addition and subtraction. "AND", "ORR" and "EOR" are logical operations which indicate AND, OR and, Exclusive OR respectively. "END" ends program and enters into sleep mode for power saving purpose.

5.2. I/O Description

SPES II has the following I/O pins: RESET, TG1, TG2, TG3, TG4, STOP [0:7]. The RESET, TG1, TG2, TG3 and TG4 are input pins and STOP [0:7] are output pins; moreover, STOP [6:7] can be shared with LED drive pins.

PIN	Configuration
RESET	Input
TG1	Input
TG2	Input
TG3	Input
TG4	Input
STOP.0	Output
STOP.1	Output
STOP.2	Output
STOP.3	Output
STOP.4	Output
STOP.5	Output
STOP.6	Output (shared with LED2 pin)
STOP.7	Output (shared with LED1 pin)

5.3. Program Structure Overview

The following description is an overview of SPES II program structure. For more information about SPES II programming method, please refer to SPES II Programming Guide.

5.3.1. Definition area

The beginning of a program is the Definition Area that defines some declarations before Initialization such as IC body, variable, frequency, debounce time and low voltage reset option.

5.3.1.1. IC body

The first element defined in a program is a SPES II body.

Example:

```
          SPES204B        ;select SPES204B
          EXT_CLK_4M
          Freq4           ;Set default speech
                          ;sample frequency to 7.8K
          LVR_DISABLE
          ...
     POI:
          ...
          ...
```

5.3.1.2. Debounce

A key debounce time can be defined in Definition Area. The range of debounce time is 5ms ~ 35ms.

5.3.1.3. Variable

A variable can be defined by adding a "#define" in front of a variable. A variable can be the combination of numbers and characters, but not underscore.

Variable Syntax:

```
#define  VariableName  <Register | NUM>
```

Example1:

```
#define var  R0       ;define var as R0
```

Example2:

```
#define const 8     ;define const as 8
```

5.3.1.4. External clock

Users can define one external clock out of the following selections in a program. This option must be defined in definition area.

EXT_CLK_3M; (3.0MHz)

EXT_CLK_4M; (4.0MHz)

EXT_CLK_6M; (6.0MHz)

5.3.1.5. Low voltage reset

The SPES204B provides Low Voltage Reset (LVR) function that will reset all functions into the initial state if the VDD power drops below 1.4V for longer than one clock cycle. As a result, it prevents the SPES204B entering into a malfunction state. The LVR function is the same as Power ON Reset.

The Low Voltage Reset can be enabled or disabled in a program. This option must be defined in definition area.

LVR_ENABLE; enable
LVR_DISABLE; disable

5.3.1.6. Infrared Red (IR) function

Some IR parameters must be defined in Definition Area before using IR function. We will only introduce the commands here. For more details on how to use these commands in your program, please refer to SPES II Programming Guide.

5.3.2. Entry point (Label)

The essence applied in SPES II is the ENTRY POINT. Each trigger pin is assigned an entry point. *Instructions must be located in a new line under its entry point. Any instruction located with the same line as entry point will cause error when compiling.* Users can also define a label (ID) for an entry point. A label can be the combinations of number and character, but not underscore. In addition, a label can not start with a number.

Example:

```
SpeechLoop:
            Sound1+Sound2
            JP  SpeechLoop
```

When a pin is triggered, the program jumps to its corresponding entry point and starts executing. The entry points are fixed values. For instance, '0' is the entry point of TG1 when 1→0. '1' is the entry point of TG2 when 1→0. Users can either use Entry Point ID or Entry Point Abbreviator to express an entry point. A summary of entry point for each trigger pin is as follows:

Entry Point	Entry Point Abbreviator	Status
32	POI	Power on initialization
0	TG1F	TG1 1→0 (falling)
1	TG2F	TG2 1→0 (falling)
2	TG3F	TG3 1→0 (falling)
3	TG4F	TG4 1→0 (falling)
4	TG1R	TG1 0→1 (rising)
5	TG2R	TG2 0→1 (rising)
6	TG3R	TG3 0→1 (rising)
7	TG4R	TG4 0→1 (rising)
8 ~ 253 (except 32)	User-Defined entry point or label	User-Defined
254	*Speech event*	*User-Defined*
255	*Timer event*	*User-Defined*

Example:

An example is introduced here. Also, all words after semi-colon (;) are for comments only.

```
        SPES204B                 ;body defined
        EXT_CLK_4M
        LVR_Disable
    POI:
        LD  EN, 0x00
        (4000)_3
        LD  EN, 0x 03            ;enable TG1 falling and
                                 ;TG2 falling
        END

    TG1F:
        Sound1                   ;when TG1 changes from
                                 ;1→0 (High→Low),
                                 ;sound1 is played
        END                      ;Sleep

    TG2F:
        Sound2                   ;when TG2 changes from
                                 ;1→0, sound2 is played
        END                      ;Sleep
```

DATA SHEET

SUNPLUS

SPC11024A

One Channel Sound Controller with 24K-byte ROM

Preliminary

MAY. 26, 2005

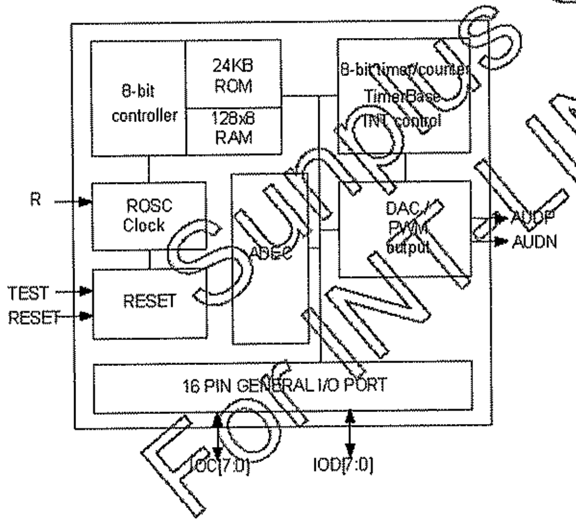
Version 0.1

ONE CHANNEL SOUND CONTROLLER WITH 24K-BYTE ROM

1. GENERAL DESCRIPTION

The SPC11024A, a one-channel speech/two-channel wave table synthesizer, equips an 8-bit CMOS microprocessor, and 24K-byte Working ROM, 128-byte working SRAM. Other primary features include two 8-bit Timer/Counters and can cascade to one 16-bit timer/counter, 16 Software Selectable I/Os, One 8-bit DAC and a pair of PWM output. It operates at a wide voltage range of 2.4V - 5.5V. Plus, a Clock Stop mode is built in for power savings. The unique power saving mode saves the RAM contents, but freezes the oscillator to stop executing other functions. The maximum CPU frequency can run up to 8MHz and the instruction cycle is two clock cycles (min.) ~ six clock cycles (max.). The SPC11024A loads, not only the latest technology, but also the full commitment and technical support of Sunplus.

2. BLOCK DIAGRAM



3. FEATURES

- 8-bit microprocessor
- 24K bytes ROM
- **128-byte working SRAM**
- Software-based audio processing
- Wide operating voltage: 2.4V - 3.6V @ 6.0MHz
  3.6V - 5.5V @ 8.0MHz
- **Supports ROSC only**
- Max. CPU clock: 6.0MHz @ 3.0V, 8MHz @ 5.0V
- Standby mode (Clock Stop mode) for power savings.
  Max. 2.0μA @ 5.0V
- 500ns instruction cycle time @ 4.0MHz CPU clock
- 16 general I/Os
- Two 8-bit timer/counters and can cascade to one 16-bit timer/counter
- Six INT sources
- Key wake -up function
- IR function
- External feedback input
- Watch dog function
- **One DAC and A pair of PWM output**

4. APPLICATION FIELD

- Intelligent education toys
  Ex. Pattern to voice (animal, car, color, etc.)
  Spelling (English or Chinese)
  Math
- Advanced toy controller
- General speech synthesizer
- Industrial controller

6. FUNCTIONAL DESCRIPTIONS

6.1. CPU

The microprocessor in SPC11024A is a high performance 8-bit processor equipped Accumulator, Program Counter, X and Y Register, Stack pointer and Processor Status Register (the same as the 6502 instruction structure). The maximum CPU speed of 8.0MHz is capable of bringing you the cleaner speech, pleasant music as well as achieving the best performance.

6.2. RAM Area

The total RAM size is 128-bytes (including Stack) starting from address $0080 through $00FF or mapping to $0180 through $01FF.

6.3. ROM Area

The SPC11024A provides a 24K-byte ROM that can be defined as the program area, audio data area, or both. To access ROM, users should program the BANK SELECT Register, choose bank, and access address to fetch data.

6.4. Power Saving Mode

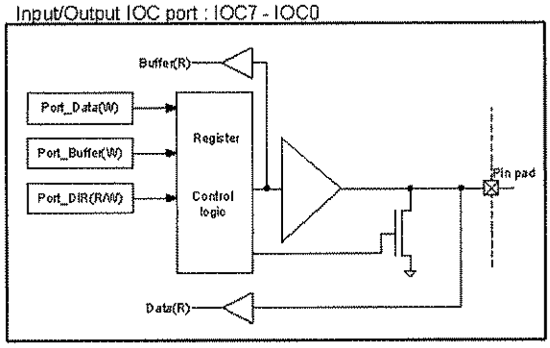
The SPC11024A includes a power saving mode (Standby mode) for those applications that require very low standby current. To enter standby mode, the Wake-Up Register must be enabled and then stop the CPU clock by writing the STOP CLOCK Register to enter standby mode. In such mode, RAM and I/Os will remain in their previous states until being awaken. Port IOD7-0 is the only wake-up source in the SPC11024A. After the SPC11024A is awaken, the internal CPU will go to the RESET State (Tw ≧ 64 x T1) and continue to execute program. Wakeup Reset will not affect RAM nor I/Os.

6.5. Map of Memory and I/Os

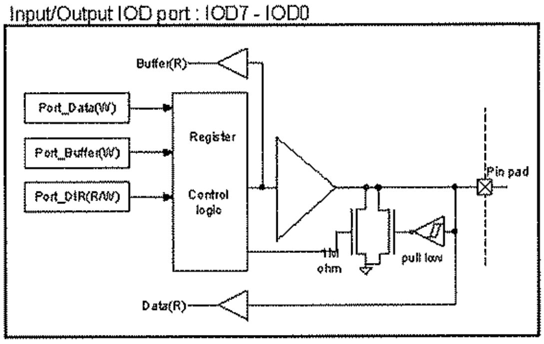
Address	Area
0x0000 – 0x0017	IO
	Reserved
0x0080 – 0x00FF	SRAM
	Reserved
0x0180 – 0x01FF	SRAM (Mapping)
	Reserved
0x0200	Test Program
0x0600 – 0x0_57FF	User's Program & Data Area
0x0_5800 – 0x0_6FFF	UNUSED
0x0_7000 – 0x0_7FFF	User's Program & Data Area

6.6. I/O Port Configuration*

Input/Output IOC port : IOC7 - IOC0



Input/Output IOD port : IOD7 - IOD0



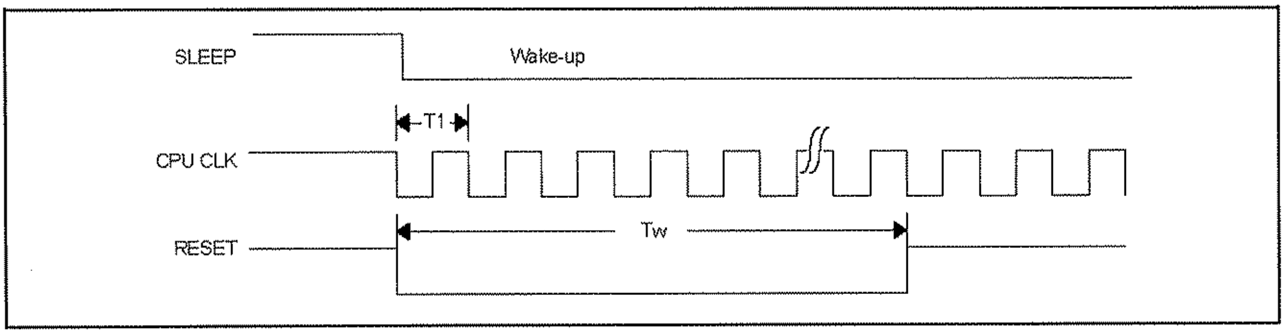
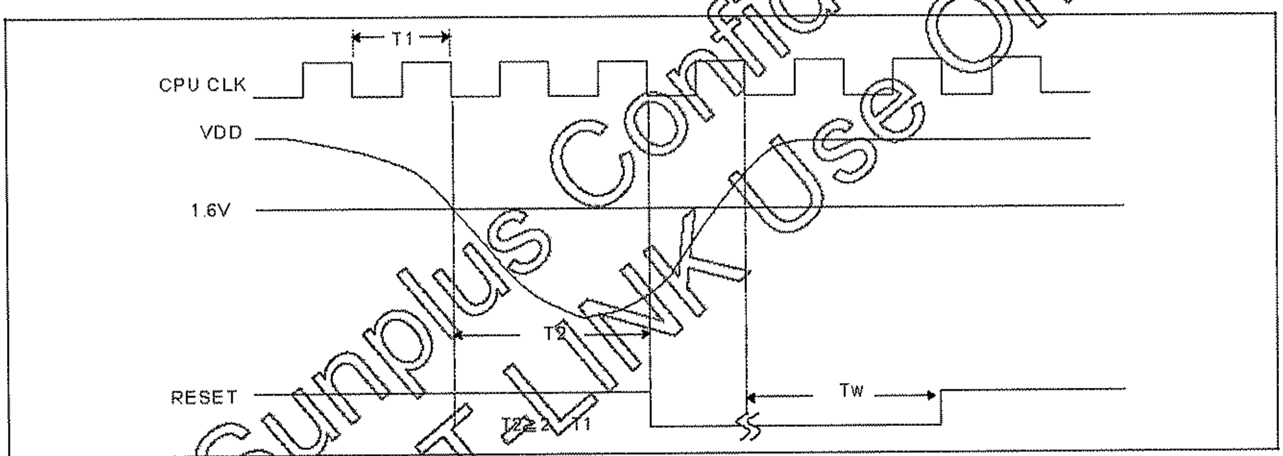


FIG. 1

T1 = 1 / (F_{CPU}), Tw ≧ 64 x T1

6.7. Low Voltage Reset

The SPC11024A has a Low Voltage Reset (LVR) function. In general, the CPU becomes unstable and malfunctions when the power voltage drops below certain operating voltage. With the unique design of Low Voltage Reset in SPC11024A, it is able to reset all functions to the initial operational (stable) state if the VDD power-supply voltage drops below 1.6V.



(The LVR function is the same as Power ON Reset or External Reset.)

6.8. Timer/Counter

The SPC11024A has two 8-bit timer/counters, TMA and TMB respectively. TMA can be specified as a timer, but TMB can be used as a timer or a counter. In the timer mode, TMA and TMB are re-loaded up-counters. When timer rollovers from $FF to $00, the carry (overflow) signal will make the user's preset value to be loaded into timer automatically and up-count again. At the same time, the carry signal will generate an INT signal if the corresponding bit is enabled in the INT ENABLE Register. Suppose TMB is specified as a counter, users can reset it by loading #0 into the counter. After the counter has been activated, the value in the counter can also be read at the same time. The read instruction will not affect the value of the counter nor reset it.

Clock source of Timer/Counter can be selected as follows:

Timer/Counter		Clock Source
TMA	8-BIT TIMER	CPU CLOCK (T) or T/8, T/64, TMB overflow
TMB	8-BIT TIMER	T, T/65536, EXTCLK, 0, 1

6.9. Speech and Melody

In speech synthesis, the SPC11024A can use NMI for accurate sampling frequency. The user can store the speech data in ROM and play it back with realistic sound quality. Several algorithms are recommended for high fidelity and compression of sound: PCM, LOG PCM, ADPCM and SACMA3400.

DATA SHEET

SUNPLUS

SPC11192A

One channel Sound Controller with 192K Bytes ROM

Preliminary

NOV. 25, 2003

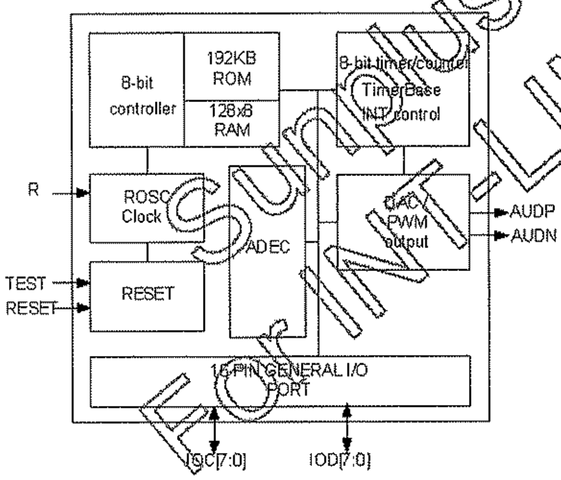
Version 0.1

ONE CHANNEL SOUND CONTROLLER WITH 192K BYTES ROM

1. GENERAL DESCRIPTION

The SPC11192A, a one-channel speech/two-channel wave table synthesizer, equips an 8-bit CMOS microprocessor, and 192K-byte Working ROM, 128-byte working SRAM. Other primary features include two 8-bit Timer/Counters and can cascade to one 16-bit timer/counter, 16 Software Selectable I/Os, One 8-bit DAC and a pair of PWM output. It operates at a wide voltage range of 2.4V - 5.5V. Plus, a Clock Stop mode is built in for power savings. The unique power saving mode saves the RAM contents, but freezes the oscillator to stop executing other functions. The maximum CPU frequency can run up to 8MHz and the instruction cycle is two clock cycles (min.) ~ six clock cycles (max.). The SPC11192A loads, not only the latest technology, but also the full commitment and technical support of Sunplus.

2. BLOCK DIAGRAM



3. FEATURES

- 8-bit microprocessor
- 192K bytes ROM
- **128-byte working SRAM**
- Software-based audio processing
- Wide operating voltage: 2.4V - 5.5V @ 6.0MHz
  3.0V - 5.5V @ 8.0MHz
- **Supports ROSC only**
- Max. CPU clock: 6MHz @ 3.0V, 10MHz @ 5.0V
- Standby mode (Clock Stop mode) for power savings.
  Max. 2.0uA @ 5.0V
- 500ns instruction cycle time @ 4.0MHz CPU clock
- **16 general I/Os**
- Two 8-bit timer/counters and can cascade to one 16-bit timer/counter
- Six INT sources
- Key wake-up function
- IR function
- External feedback input
- Watch dog function
- **One DAC and A pair of PWM output**

4. APPLICATION FIELD

- Intelligent education toys
  Ex. Pattern to voice (animal, car, color, etc.)
  Spelling (English or Chinese)
  Math
- Advanced toy controller
- General speech synthesizer
- Industrial controller

6. FUNCTIONAL DESCRIPTIONS

6.1. CPU

The microprocessor in SPC11192A is a high performance 8-bit processor equipped Accumulator, Program Counter, X and Y Register, Stack pointer and Processor Status Register (the same as the 6502 instruction structure). The maximum CPU speed of 8.0MHz is capable of bringing you the cleaner speech, pleasant music as well as achieving the best performance.

6.2. RAM Area

The total RAM size is 128-bytes (including Stack) starting from address $0080 through $00FF or mapping to $0180 through $01FF.

6.3. ROM Area

The SPC11192A provides a 192K-byte ROM that can be defined as the program area, audio data area, or both. To access ROM, users should program the BANK SELECT Register, choose bank, and access address to fetch data.

6.4. Power Saving Mode

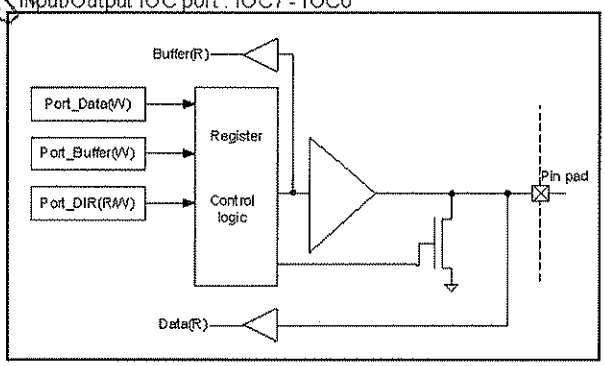
The SPC11192A includes a power saving mode (Standby mode) for those applications that require very low standby current. To enter standby mode, the Wake-Up Register must be enabled and then stop the CPU clock by writing the STOP CLOCK Register to enter standby mode. In such mode, RAM and I/Os will remain in their previous states until being awaken. Port IOD7-0 is the only wake-up source in the SPC11192A. After the SPC11192A is awaken, the internal CPU will go to the RESET State (Tw ≥ 64 x T1) and continue to execute program. Wakeup Reset will not affect RAM nor I/Os.

6.5. Map of Memory and I/Os

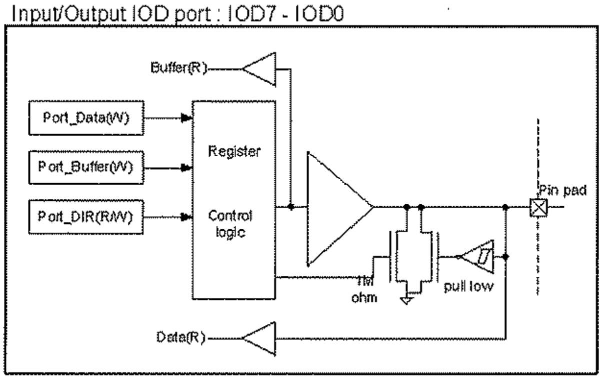
Address	Area
0x0000 – 0x0017	IO
	Reserved
0x0080 – 0x00FF	SRAM
	Reserved
0x0180 – 0x01FF	SRAM (Mapping)
	Reserved
0x0200	Test Program
0x0600 – 0x2_FFFF	User's Program & Data Area

6.6. I/O Port Configuration*

Input/Output IOC port : IOC7 - IOC0



Input/Output IOD port : IOD7 - IOD0



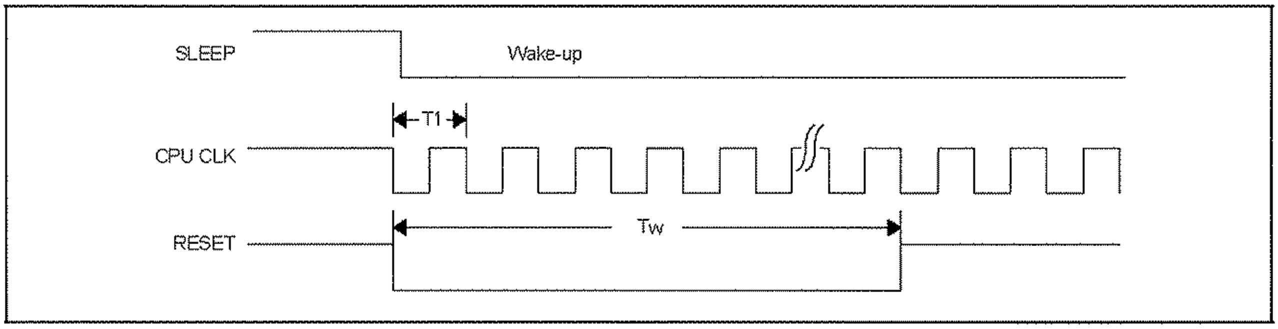


FIG. 1

T1 = 1 / (F_{CPU}), Tw ≧64 x T1

6.7. Timer/Counter

The SPC11192A has two 8-bit timer/counters, TMA and TMB respectively. TMA can be specified as a timer, but TMB can be used as a timer or a counter. In the timer mode, TMA and TMB are re-loaded up-counters. When timer rollovers from $FF to $00, the carry (overflow) signal will make the user's preset value to be loaded into timer automatically and up-count again. At the same time, the carry signal will generate an INT signal if the corresponding bit is enabled in the INT ENABLE Register. Suppose TMB is specified as a counter, users can reset it by loading #0 into the counter. After the counter has been activated, the value in the counter can also be read at the same time. The read instruction will not affect the value of the counter nor reset it.

Clock source of Timer/Counter can be selected as follows:

Timer/Counter		Clock Source
TMA	8-BIT TIMER	CPU CLOCK (T) or T/8, T/64, TMB overflow
TMB	8-BIT TIMER	T, T/65536, EXTCLK, 0, 1

6.8. Speech and Melody

In speech synthesis, the SPC11192A can use NMI for accurate sampling frequency. The user can store the speech data in ROM and play it back with realistic sound quality. Several algorithms are recommended for high fidelity and compression of sound: PCM, LOG PCM, ADPCM and SACMA3400.

DATA SHEET

SUNPLUS

SPRC205A/SPRC206A

5-Function Remote Control Encoder/Decoder

Preliminary

MAR. 14, 2005

Version 0.3

FIVE FUNCTIONS REMOTE CONTROL ENCODER/DECODER PAIRS

1. GENERAL DESCRIPTION

These two devices are especially designed is use as paired encoder/decoder in remote control (RC) applications.

The SPRC205A, a RC encoder, is able to encode five lines of binary information into a serial bit-stream data. When any of the 5-line information is activated, built-in crystal oscillator and power amplifier will be enabled to deliver the encoded bit-stream data. After the 5-line information becomes inactive, the SPRC205A will transmit additional fifteen data frames to increase transmission reliability.

The SPRC206A is a remote control decoder, which decodes the serial bit-stream data received from the SPRC205A and interprets the 5-line information as 5-bit output data to control the corresponding external component. The SPRC206A will be activated only when two consecutive and equal frames are received.

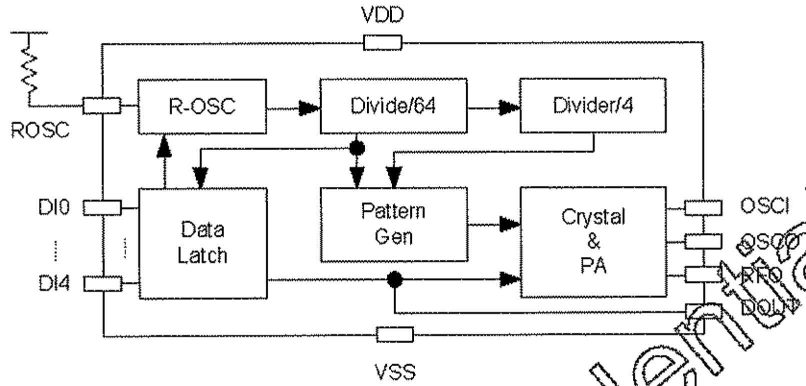
With SUNPLUS state-of-the-art technology and strong support, SPRC205A and SPRC206A are the simplest and most suitable products for your RC products.

2. FEATURES

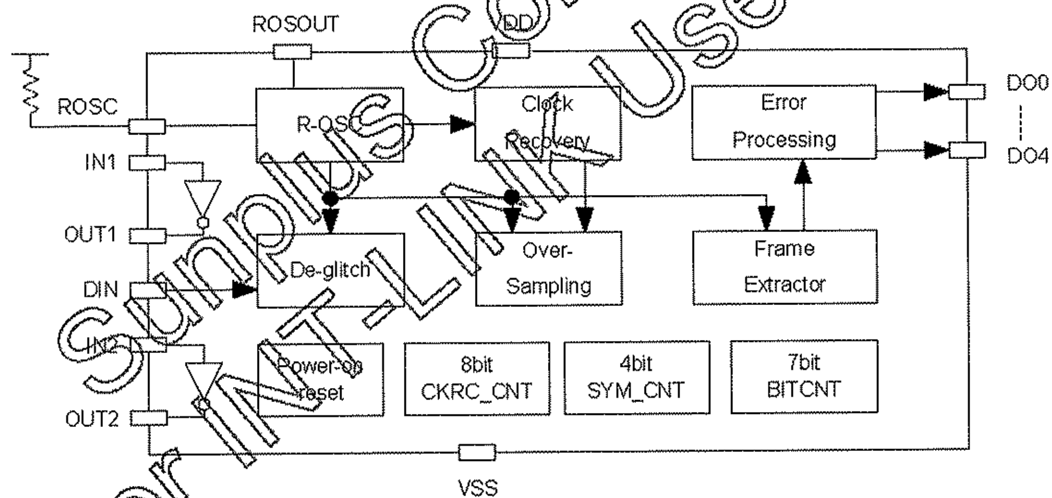
- Operating voltage
  - 2.2V - 5.5V operation
- Built-in R-oscillator (a 5% resistor required)
- Low standby and operating current
  - $I_{STBY,SPRC206A} < 1.0\mu A$, R-oscillator stops
  - $I_{OPERATE,SPRC205A} < 15mA$, R-oscillator free run, crystal & PA on
  - $I_{OPERATE,SPRC206A} < 100\mu A$, R-oscillator free run
- Built-in power on reset
- Built-in Crystal & PA in SPRC205A
- 5-function I/O pins
- $2^5 = 32$ encoding in SPRC205A
- Variable frame rates controlled by external resistor

3. BLOCK DIAGRAM

SPRC205A



SPRC206A



5. FUNCTIONAL DESCRIPTIONS

5.1. Frame Format

Preamble						PO	E	D0	D1	D2	D3	D4
P	P	P	P	P	P	A/I	A/I	A/I	A/I	A/I	A/I	A/I

Preamble field: 6 preamble fields

PO field: Even parity check field

E field: Frame polarity indication field; frames are transmitted in positive/negative sequence.

Data field: 5 data fields

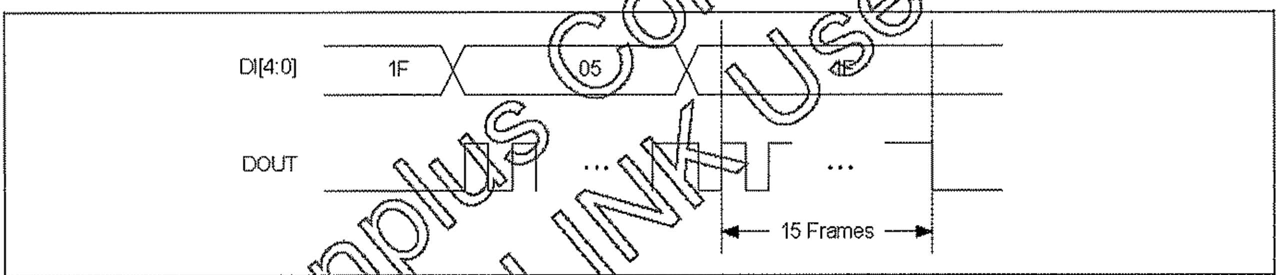
P pattern: encoded as 101

A pattern: encoded as 100

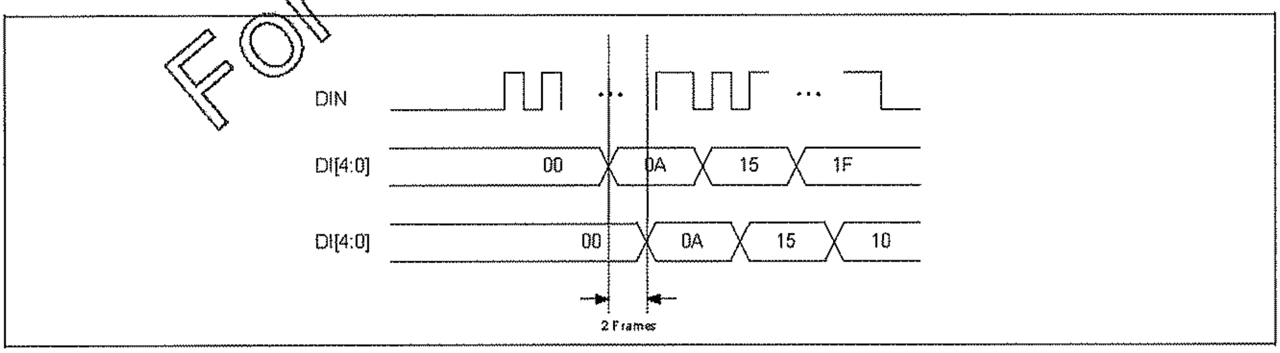
I pattern: encoded as 110

5.2. Operation

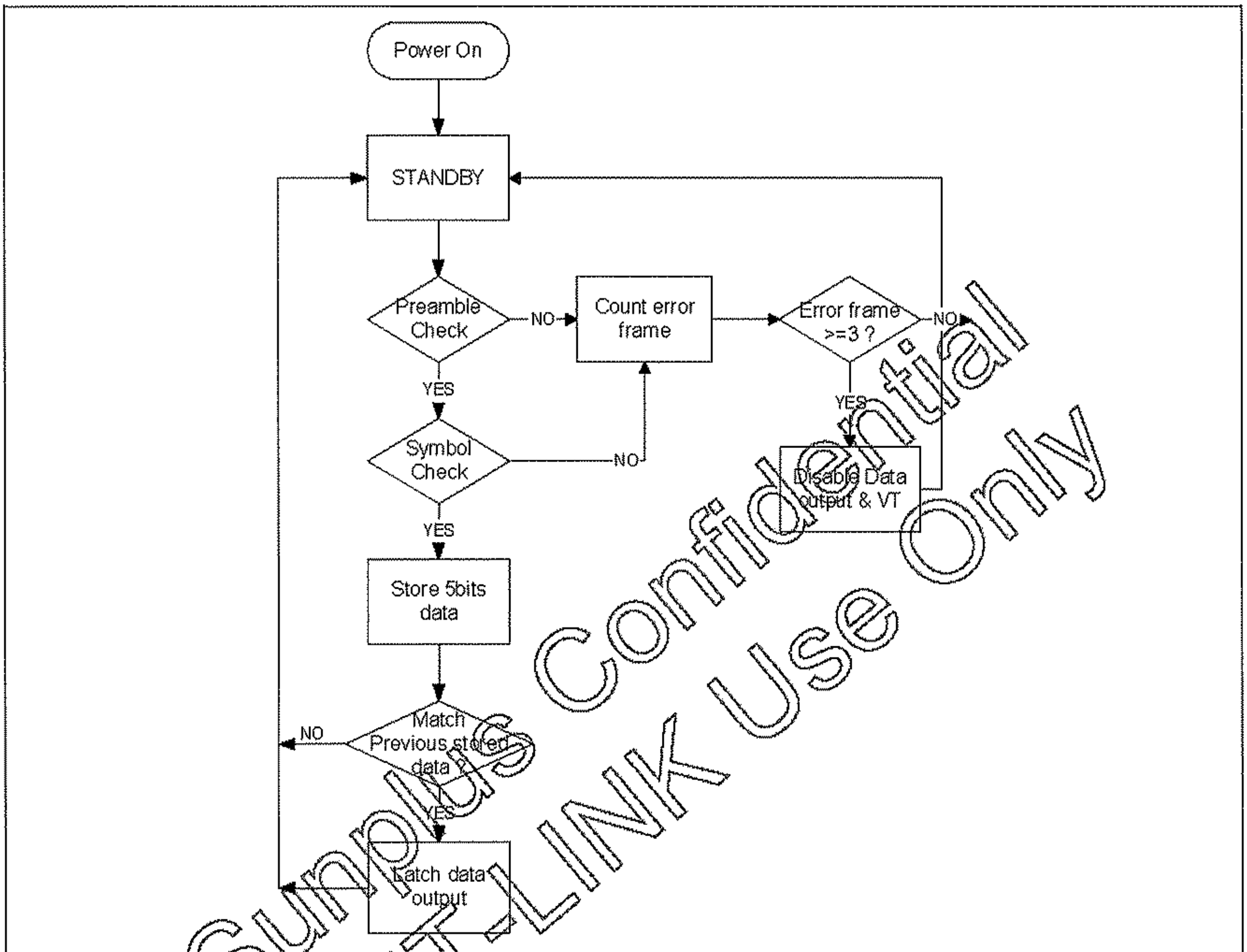
The SPRC205A encodes 5-function information into 2^5 series of bit-stream data and transmits the encoded data stream via RFO when any of the 5-function I/Os is activated. The cycle will repeat until all 5-function I/Os become inactive. After these 5-function I/Os become inactive, SPRC205A will transmit another 15 all-zero frames to inform SPRC206A returning to disabled state. The transmitting timing is shown as follows:



The SPRC206A is able to receive serial bit-stream data transmitted from SPRC205A and decode the data fields as 5-bits data output. Any signal on DIN pin will activate SPRC206A to decode the incoming data. When SPRC206A receives two consecutive, correct and equal frames, DO[4:0] is able to control the external component. The DO[1,0] and DO[3:2] are exclusive to each other; that is, DO[1:0] and DO[3:2] cannot be activated at the same time. The receiving timing is shown below:



5.3. Decoder Flow Chart



After power on, it is reset at STANDBY state. When the signal on DIN is received by SPRC206A, it will check the incoming data frame structure. If preamble or data field errors occur, it will back to STANDBY state to check the next frame. If the receiving frame structure passes the preamble and symbol checks, the 5-bit data is stored and then compared to the previous stored 5-bits data. If the present data matches the previous data, DO[4:0] is active and it is back to STANDBY and ready to check the next frame.

5.4. R-oscillator

Both SPRC205A and SPRC206A have built in R-oscillator. Users need only one resistor (or a capacitor if needed) to implement the clock input and to change the frame rate by replacing different resistor.

Frame rate = F_{OSC} / 64 / 33

In addition, the SPRC206A built-in a Clock Recovery block to automatically adjust the ratio of data rate to clock rate. The only limitation is using a 5% accuracy resistor is required in SPRC205A and SPRC206A.

5.5. Super Regeneration Amplifier

The SPRC206A features two inverter inputs and outputs as pins. The two inverters can be used for amplifier of the Super-Regeneration RF receiver data output. Users can change the two inverters' gain by adjusting external resistor and capacitor.

DATA SHEET

SUNPLUS

SPES204B

easy-to-use SOUNDPLUS

Preliminary

MAY. 06, 2003

Version 0.2

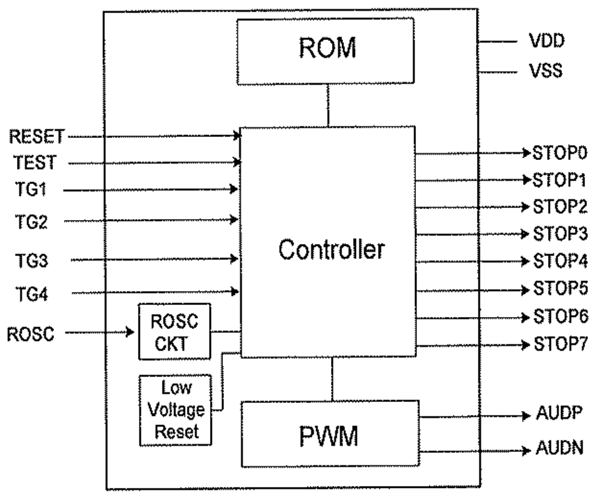
easy-to-use SOUNDPLUS

1. GENERAL DESCRIPTION

The easy-to-use SOUNDPLUS II (SPESII) is an enhanced version of easy-to-use SOUNDPLUS (SPES). Many features such as infrared Red (IR) have been added in SPES II to increase its capability and performance. One of the most significant features in SPES II is that no complex program structure is necessary. With only nine instructions and six registers, SPES II is capable of driving sophisticated tasks and playing realistic sound with simple program structure. Programmer can easily implement application rapidly and increase productivity efficiently.

The SPES204B, one of the SPES II families, stores up to 4 seconds of sound data (@ 6.0KHz sample rate). It also contains four trigger pins, eight output pins, PWM audio output, and five LED flash alternations. To assure the system reliability, a watchdog and a Low Voltage Reset (LVR) are also built in for monitoring possible critical conditions. With the high cost/performance ratio, SPES204B is one of the most suitable engines in the industry for vocal products.

2. BLOCK DIAGRAM



3. FEATURES

- 16KB ROM SIZE
- Programmable speech synthesizer
- Operating voltage:
  - 2.4V - 5.5V for 4.0MHz operating clock
  - 3.6V - 5.5V for 6.0MHz operating clock
- 4 direct trigger inputs that can be extended to 36 matrix key
- Up to 8 programmable outputs
- Programmable power on initialization
- 256 voice group entries available
- Mask options: Trigger input debounce time from 5ms to 35ms
- Flexible functions through the following:
  - LD (load), JP (jump) commands
  - 6 registers: R0, R1, R2, R3, EN, STOP
  - Conditional instructions
  - Speech equation
  - END instruction
  - Local repeat setting
  - Output frequency and LED flash type setting
- Approx. 4 sec. speech (6.0KHz sample rate)
- Low voltage reset function
- Watchdog function
- A pair of PWM outputs
- Flexible functions as the follows:
  - Interrupt or non-interrupt for rising or falling edge of each trigger.
  - Eight programmable playing modes:
    - One shot
    - Level hold
    - Single-cycle level hold
    - Complete-cycle level hold
    - Sequence
    - Level-Auto
    - Random
    - Non-retrigger
  - Stop signal output setting
- Each voice section provides
  - Programmable sampling frequency:
    - 2K to 10K for 4.0MHz operating clock
    - 2K to 15K for 6.0MHz operating clock
  - Five LED flash type : On, Off, Alternatively, Synchronous, Volume-controlled
  - LED: programmable
- Infrared Red (IR) communication Function
- Play Speech with tags. Seven different tags are available

5. FUNCTIONAL DESCRIPTIONS

5.1. Instruction Sets

Nine instructions involve *LD, JP, LSR, ADD, SUB, AND, ORR, EOR, and END*. "LD" represents LOAD and "JP" indicates JUMP. "LSR" shifts a register's value one bit to the right. "ADD" and "SUB" are addition and subtraction. "AND", "ORR" and "EOR" are logical operations which indicate AND, OR and, Exclusive OR respectively. "END" ends program and enters into sleep mode for power saving purpose.

5.2. I/O Description

SPES II has the following I/O pins: RESET, TG1, TG2, TG3, TG4, STOP [0:7]. The RESET, TG1, TG2, TG3 and TG4 are input pins and STOP [0:7] are output pins; moreover, STOP [6:7] can be shared with LED drive pins.

PIN	Configuration
RESET	Input
TG1	Input
TG2	Input
TG3	Input
TG4	Input
STOP.0	Output
STOP.1	Output
STOP.2	Output
STOP.3	Output
STOP.4	Output
STOP.5	Output
STOP.6	Output (shared with LED2 pin)
STOP.7	Output (shared with LED1 pin)

5.3. Program Structure Overview

The following description is an overview of SPES II program structure. For more information about SPES II programming method, please refer to SPES II Programming Guide.

5.3.1. Definition area

The beginning of a program is the Definition Area that defines some declarations before Initialization such as IC body, variable, frequency, debounce time and low voltage reset option.

5.3.1.1. IC body

The first element defined in a program is a SPES II body.

Example:

```
          SPES204B        ;select SPES204B
          EXT_CLK_4M
          Freq4           ;Set default speech
                          ;sample frequency to 7.8K
          LVR_DISABLE
          ...
     POI:
          ...
          ...
```

5.3.1.2. Debounce

A key debounce time can be defined in Definition Area. The range of debounce time is 5ms ~ 35ms.

5.3.1.3. Variable

A variable can be defined by adding a "#define" in front of a variable. A variable can be the combination of numbers and characters, but not underscore.

Variable Syntax:

```
    #define  VariableName  <Register | NUM>
```

Example1:

```
        #define var  R0       ;define var as R0
```

Example2:

```
        #define const  8      ;define const as 8
```

5.3.1.4. External clock

Users can define one external clock out of the following selections in a program. This option must be defined in definition area.

EXT_CLK_3M; (3.0MHz)
EXT_CLK_4M; (4.0MHz)
EXT_CLK_6M; (6.0MHz)

5.3.1.5. Low voltage reset

The SPES204B provides Low Voltage Reset (LVR) function that will reset all functions into the initial state if the VDD power drops below 1.4V for longer than one clock cycle. As a result, it prevents the SPES204B entering into a malfunction state. The LVR function is the same as Power ON Reset.

The Low Voltage Reset can be enabled or disabled in a program. This option must be defined in definition area.

LVR_ENABLE; enable
LVR_DISABLE; disable

5.3.1.6. Infrared Red (IR) function

Some IR parameters must be defined in Definition Area before using IR function. We will only introduce the commands here. For more details on how to use these commands in your program, please refer to SPES II Programming Guide.

5.3.2. Entry point (Label)

The essence applied in SPES II is the ENTRY POINT. Each trigger pin is assigned an entry point. *Instructions must be located in a new line under its entry point. Any instruction located with the same line as entry point will cause error when compiling.* Users can also define a label (ID) for an entry point. A label can be the combinations of number and character, but not underscore. In addition, a label can not start with a number.

Example:

```
SpeechLoop:
        Sound1+Sound2
        JP  SpeechLoop
```

When a pin is triggered, the program jumps to its corresponding entry point and starts executing. The entry points are fixed values. For instance, '0' is the entry point of TG1 when 1→0. '1' is the entry point of TG2 when 1→0. Users can either use Entry Point ID or Entry Point Abbreviator to express an entry point. A summary of entry point for each trigger pin is as follows:

Entry Point	Entry Point Abbreviator	Status
32	POI	Power on initialization
0	TG1F	TG1 1→0 (falling)
1	TG2F	TG2 1→0 (falling)
2	TG3F	TG3 1→0 (falling)
3	TG4F	TG4 1→0 (falling)
4	TG1R	TG1 0→1 (rising)
5	TG2R	TG2 0→1 (rising)
6	TG3R	TG3 0→1 (rising)
7	TG4R	TG4 0→1 (rising)
8 ~ 253 (except 32)	User-Defined entry point or label	User-Defined
254	*Speech event*	*User-Defined*
255	*Timer event*	*User-Defined*

Example:
An example is introduced here. Also, all words after semi-colon (;) are for comments only.

```
        SPES204B                    ;body defined
        EXT_CLK_4M
        LVR_Disable
    POI:
        LD  EN, 0x00
        (4000)_3
        LD  EN, 0x 03               ;enable TG1 falling and
                                    ;TG2 falling
        END

    TG1F:
        Sound1                      ;when TG1 changes from
                                    ;1→0 (High→Low),
                                    ;sound1 is played
        END                         ;Sleep

    TG2F:
        Sound2                      ;when TG2 changes from
                                    ;1→0, sound2 is played
        END                         ;Sleep
```

DATA SHEET

SUNPLUS

SPC11024A

One Channel Sound Controller with 24K-byte ROM

Preliminary

MAY. 26, 2005

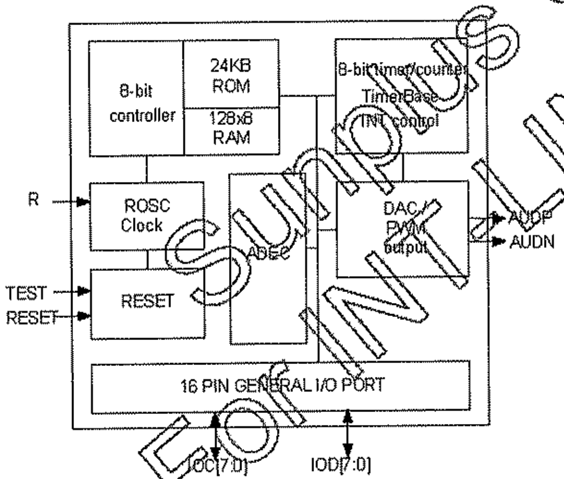
Version 0.1

ONE CHANNEL SOUND CONTROLLER WITH 24K-BYTE ROM

1. GENERAL DESCRIPTION

The SPC11024A, a one-channel speech/two-channel wave table synthesizer, equips an 8-bit CMOS microprocessor, and 24K-byte Working ROM, 128-byte working SRAM. Other primary features include two 8-bit Timer/Counters and can cascade to one 16-bit timer/counter, 16 Software Selectable I/Os, One 8-bit DAC and a pair of PWM output. It operates at a wide voltage range of 2.4V - 5.5V. Plus, a Clock Stop mode is built in for power savings. The unique power saving mode saves the RAM contents, but freezes the oscillator to stop executing other functions. The maximum CPU frequency can run up to 8MHz and the instruction cycle is two clock cycles (min.) ~ six clock cycles (max.). The SPC11024A loads, not only the latest technology, but also the full commitment and technical support of Sunplus.

2. BLOCK DIAGRAM



3. FEATURES

- 8-bit microprocessor
- 24K bytes ROM
- **128-byte working SRAM**
- Software-based audio processing
- Wide operating voltage: 2.4V - 3.6V @ 6.0MHz
  3.6V - 5.5V @ 8.0MHz
- **Supports ROSC only**
- Max. CPU clock: 6.0MHz @ 3.0V, 8MHz @ 5.0V
- Standby mode (Clock Stop mode) for power savings.
  Max. 2.0μA @ 5.0V
- 500ns instruction cycle time @ 4.0MHz CPU clock
- 16 general I/Os
- Two 8-bit timer/counters and can cascade to one 16-bit timer/counter
- Six INT sources
- Key wake -up function
- IR function
- External feedback input
- Watch dog function
- **One DAC and A pair of PWM output**

4. APPLICATION FIELD

- Intelligent education toys
  Ex. Pattern to voice (animal, car, color, etc.)
  Spelling (English or Chinese)
  Math
- Advanced toy controller
- General speech synthesizer
- Industrial controller

6. FUNCTIONAL DESCRIPTIONS

6.1. CPU

The microprocessor in SPC11024A is a high performance 8-bit processor equipped Accumulator, Program Counter, X and Y Register, Stack pointer and Processor Status Register (the same as the 6502 instruction structure). The maximum CPU speed of 8.0MHz is capable of bringing you the cleaner speech, pleasant music as well as achieving the best performance.

6.2. RAM Area

The total RAM size is 128-bytes (including Stack) starting from address $0080 through $00FF or mapping to $0180 through $01FF.

6.3. ROM Area

The SPC11024A provides a 24K-byte ROM that can be defined as the program area, audio data area, or both. To access ROM, users should program the BANK SELECT Register, choose bank, and access address to fetch data.

6.4. Power Saving Mode

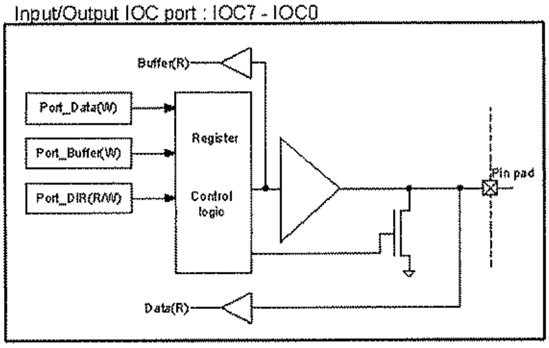
The SPC11024A includes a power saving mode (Standby mode) for those applications that require very low standby current. To enter standby mode, the Wake-Up Register must be enabled and then stop the CPU clock by writing the STOP CLOCK Register to enter standby mode. In such mode, RAM and I/Os will remain in their previous states until being awaken. Port IOD7-0 is the only wake-up source in the SPC11024A. After the SPC11024A is awaken, the internal CPU will go to the RESET State (Tw ≧ 64 x T1) and continue to execute program. Wakeup Reset will not affect RAM nor I/Os.

6.5. Map of Memory and I/Os

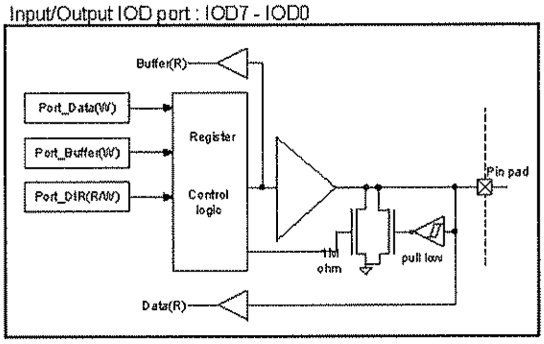
Address	Area
0x0000 – 0x0017	IO
	Reserved
0x0080 – 0x00FF	SRAM
	Reserved
0x0180 – 0x01FF	SRAM (Mapping)
	Reserved
0x0200	Test Program
0x0600 – 0x0_57FF	User's Program & Data Area
0x0_5800 – 0x0_6FFF	UNUSED
0x0_7000 – 0x0_7FFF	User's Program & Data Area

6.6. I/O Port Configuration*

Input/Output IOC port : IOC7 - IOC0



Input/Output IOD port : IOD7 - IOD0



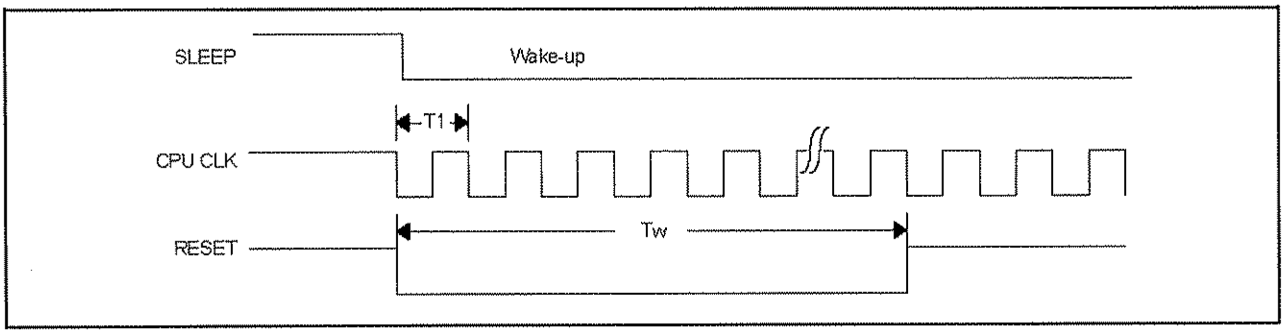
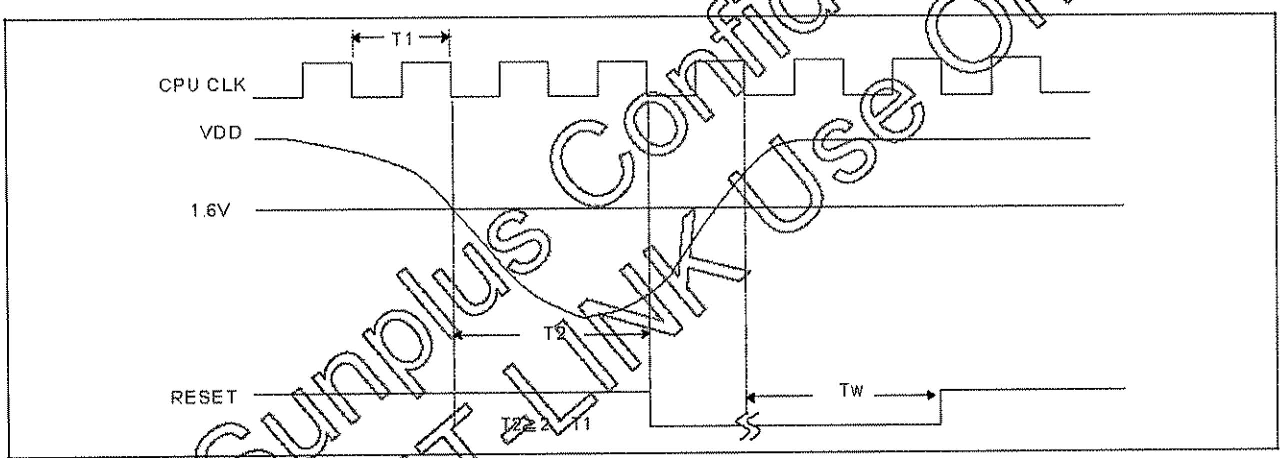


FIG. 1

$T1 = 1 / (F_{CPU})$, $Tw \geqq 64 \times T1$

6.7. Low Voltage Reset

The SPC11024A has a Low Voltage Reset (LVR) function. In general, the CPU becomes unstable and malfunctions when the power voltage drops below certain operating voltage. With the unique design of Low Voltage Reset in SPC11024A, it is able to reset all functions to the initial operational (stable) state if the VDD power-supply voltage drops below 1.6V.



(The LVR function is the same as Power ON Reset or External Reset.)

6.8. Timer/Counter

The SPC11024A has two 8-bit timer/counters, TMA and TMB respectively. TMA can be specified as a timer, but TMB can be used as a timer or a counter. In the timer mode, TMA and TMB are re-loaded up-counters. When timer rollovers from $FF to $00, the carry (overflow) signal will make the user's preset value to be loaded into timer automatically and up-count again. At the same time, the carry signal will generate an INT signal if the corresponding bit is enabled in the INT ENABLE Register. Suppose TMB is specified as a counter, users can reset it by loading #0 into the counter. After the counter has been activated, the value in the counter can also be read at the same time. The read instruction will not affect the value of the counter nor reset it.

Clock source of Timer/Counter can be selected as follows:

Timer/Counter		Clock Source
TMA	8-BIT TIMER	CPU CLOCK (T) or T/8, T/64, TMB overflow
TMB	8-BIT TIMER	T, T/65536, EXTCLK, 0, 1

6.9. Speech and Melody

In speech synthesis, the SPC11024A can use NMI for accurate sampling frequency. The user can store the speech data in ROM and play it back with realistic sound quality. Several algorithms are recommended for high fidelity and compression of sound: PCM, LOG PCM, ADPCM and SACMA3400.

DATA SHEET

SUNPLUS

SPC11192A

One channel Sound Controller with 192K Bytes ROM

Preliminary

NOV. 25, 2003

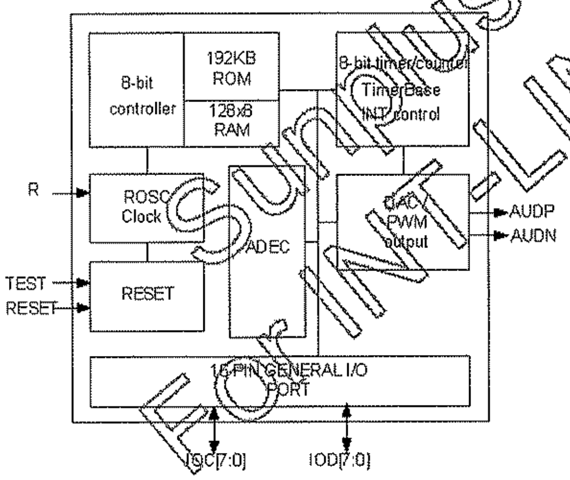
Version 0.1

ONE CHANNEL SOUND CONTROLLER WITH 192K BYTES ROM

1. GENERAL DESCRIPTION

The SPC11192A, a one-channel speech/two-channel wave table synthesizer, equips an 8-bit CMOS microprocessor, and 192K-byte Working ROM, 128-byte working SRAM. Other primary features include two 8-bit Timer/Counters and can cascade to one 16-bit timer/counter, 16 Software Selectable I/Os, One 8-bit DAC and a pair of PWM output. It operates at a wide voltage range of 2.4V - 5.5V. Plus, a Clock Stop mode is built in for power savings. The unique power saving mode saves the RAM contents, but freezes the oscillator to stop executing other functions. The maximum CPU frequency can run up to 8MHz and the instruction cycle is two clock cycles (min.) ~ six clock cycles (max.). The SPC11192A loads, not only the latest technology, but also the full commitment and technical support of Sunplus.

2. BLOCK DIAGRAM



3. FEATURES

- 8-bit microprocessor
- 192K bytes ROM
- **128-byte working SRAM**
- Software-based audio processing
- Wide operating voltage: 2.4V - 5.5V @ 6.0MHz
  3.6V - 5.5V @ 8.0MHz
- **Supports ROSC only**
- Max. CPU clock: 6MHz @ 3.0V, 10MHz @ 5.0V
- Standby mode (Clock Stop mode) for power savings.
  Max. 2.0uA @ 5.0V
- 500ns instruction cycle time @ 4.0MHz CPU clock
- **16 general I/Os**
- Two 8-bit timer/counters and can cascade to one 16-bit timer/counter
- Six INT sources
- Key wake-up function
- IR function
- External feedback input
- Watch dog function
- **One DAC and A pair of PWM output**

4. APPLICATION FIELD

- Intelligent education toys
  Ex. Pattern to voice (animal, car, color, etc.)
  Spelling (English or Chinese)
  Math
- Advanced toy controller
- General speech synthesizer
- Industrial controller

6. FUNCTIONAL DESCRIPTIONS

6.1. CPU

The microprocessor in SPC11192A is a high performance 8-bit processor equipped Accumulator, Program Counter, X and Y Register, Stack pointer and Processor Status Register (the same as the 6502 instruction structure). The maximum CPU speed of 8.0MHz is capable of bringing you the cleaner speech, pleasant music as well as achieving the best performance.

6.2. RAM Area

The total RAM size is 128-bytes (including Stack) starting from address $0080 through $00FF or mapping to $0180 through $01FF.

6.3. ROM Area

The SPC11192A provides a 192K-byte ROM that can be defined as the program area, audio data area, or both. To access ROM, users should program the BANK SELECT Register, choose bank, and access address to fetch data.

6.4. Power Saving Mode

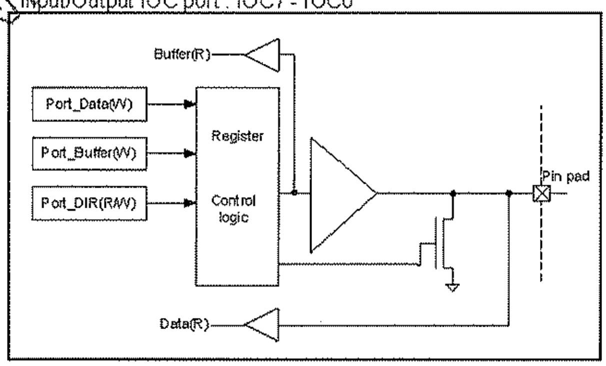
The SPC11192A includes a power saving mode (Standby mode) for those applications that require very low standby current. To enter standby mode, the Wake-Up Register must be enabled and then stop the CPU clock by writing the STOP CLOCK Register to enter standby mode. In such mode, RAM and I/Os will remain in their previous states until being awaken. Port IOD7-0 is the only wake-up source in the SPC11192A. After the SPC11192A is awaken, the internal CPU will go to the RESET State (Tw ≥ 64 x T1) and continue to execute program. Wakeup Reset will not affect RAM nor I/Os.

6.5. Map of Memory and I/Os

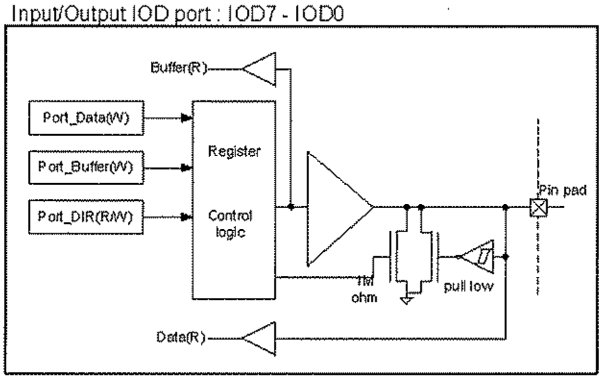
Address	Area
0x0000 – 0x0017	IO
	Reserved
0x0080 – 0x00FF	SRAM
	Reserved
0x0180 – 0x01FF	SRAM (Mapping)
	Reserved
0x0200	Test Program
0x0600 – 0x2_FFFF	User's Program & Data Area

6.6. I/O Port Configuration*

Input/Output IOC port : IOC7 - IOC0



Input/Output IOD port : IOD7 - IOD0



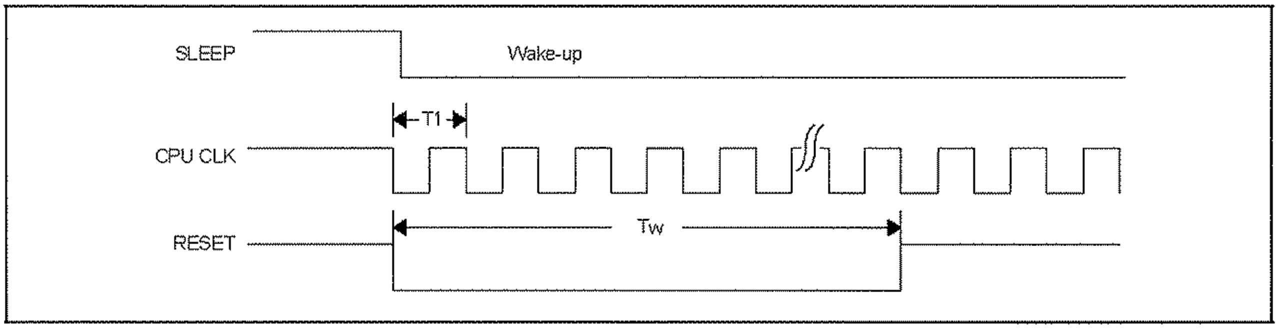


FIG. 1

T1 = 1 / (F_{CPU}), Tw ≧64 x T1

6.7. Timer/Counter

The SPC11192A has two 8-bit timer/counters, TMA and TMB respectively. TMA can be specified as a timer, but TMB can be used as a timer or a counter. In the timer mode, TMA and TMB are re-loaded up-counters. When timer rollovers from $FF to $00, the carry (overflow) signal will make the user's preset value to be loaded into timer automatically and up-count again. At the same time, the carry signal will generate an INT signal if the corresponding bit is enabled in the INT ENABLE Register. Suppose TMB is specified as a counter, users can reset it by loading #0 into the counter. After the counter has been activated, the value in the counter can also be read at the same time. The read instruction will not affect the value of the counter nor reset it.

Clock source of Timer/Counter can be selected as follows:

Timer/Counter		Clock Source
TMA	8-BIT TIMER	CPU CLOCK (T) or T/8, T/64, TMB overflow
TMB	8-BIT TIMER	T, T/65536, EXTCLK, 0, 1

6.8. Speech and Melody

In speech synthesis, the SPC11192A can use NMI for accurate sampling frequency. The user can store the speech data in ROM and play it back with realistic sound quality. Several algorithms are recommended for high fidelity and compression of sound: PCM, LOG PCM, ADPCM and SACMA3400.