

# POSGEN

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To: Tim Harrington ([tim.harrington@fcc.gov](mailto:tim.harrington@fcc.gov))

Date: 7/28/2006

/FCC Equipment Authorization Branch

From: Dae-Sung Ha ([dsha@posgen.co.kr](mailto:dsha@posgen.co.kr))

/Lab manager of R&D Center of Posgen

CC: David Kingsolver ([davidk@midlandradio.com](mailto:davidk@midlandradio.com))

Mike Kuo ([mike.kuo@ccsemc.com](mailto:mike.kuo@ccsemc.com))

Applicant : Midland Radio Corporation

FCC ID : MMALXT300

Correspondence Reference Number : 30479

731 Confirmation Number : TC292769

Subject : Reply on Audit dated 7/26/2006

Question : Please explain compliance with 47 CFR 95.651 Crystal Control Required for GMRS equipment authorization.

Reply :

Dear Sir,

Posgen is design & R&D center of LXT-300 model owning Daxian Telecommunication Ltd. (=manufacturer of this model) which is located in China.

“The compliance with 47 CFR 95.651 Crystal Control Required” is already explained in “Theory of operation”, which is submitted when new submission same as below :

## PLL Frequency Synthesizer ( IC301 )

The PLL synthesizer of the LXT-300 consists of the signal loop PLL circuit with the reference of 6.25KHz. The IC301 PLL IC includes all the functions such as the

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reference oscillator, the driver, the phase detector, the lock detector, and the programmable divider.

At the reference oscillator, the 21.25MHz TCXO of the TCXO is connected to the pin 11 of the IC301 to oscillate the frequency of 21.25MHz. The TCXO(21.25MHz) is the temperature compensation circuit to maintain the frequency within the allowable error range even under a low temperature of -30 °C

The phase detectors send out the output power to the loop filter through 3 pin of the IC301. If the oscillation frequency of the VCO is low compared to the reference frequency, the phase detector sends out the output power in positive pulse. If the oscillation frequency of the VCO is high, phase detector sends out the output power in negative pulse. Therefore, the VCO can maintain the frequency set.

The programmable divider maintains the desired frequency with the control from the CPU. The dividing ratio, "N" to oscillate the desired frequency is as below :

$N = \text{VCO oscillation frequency} / \text{reference frequency}$

If the desired frequency is 462.5625MHz

$N = 462.5625\text{MHz} / 0.00625\text{MHz} = 74802$

**If you have further questions feel free to contact me.**

**Regards,**



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**Dae-Sung Ha**

**/Lab manager of R&D Center**

**/Posgen**